K J Somaiya Institute of Engineering and Information Technology, Sion, Mumbai

An Autonomous Institute under University of Mumbai

Autonomy Syllabus Scheme-I (2021-22)

Bachelor of Technology

in

Electronics Engineering (ETRX)

(Third Year- Semester-VI)

(With Effect from AY 2021-22)

From the Principal's Desk:

The academic reforms recently recommended by the AICTE and UGC have effectually strengthened the higher education system in India. To adhere to the status quo and enhance the academic standards and quality of engineering education further, it is essential to assimilate innovation and recurrent revision in curriculum, teaching-learning methodology, examination, and assessment system.

In congruence with it, the University of Mumbai has adapted Outcome-Based Education (OBE) system and has revised the engineering curriculum thrice in the last decade as Rev 2012, Rev 2016, and the recent Rev 2019, 'C' scheme focusing on cutting-edge technology courses.

K. J. Somaiya Institute of Engineering and Information Technology, being an autonomous institute possesses more flexibility in adapting newer approaches to reach higher levels of excellence in engineering education. This first syllabus scheme under the autonomy comprises state-of-the-art courses and laboratory sessions on emerging areas of technology. The syllabus is designed with an objective to foster the students for developing innovative solutions to real-world issues of the society and/or industry through the acquired knowledge. The induction program for the students is deliberated as per guidelines of AICTE and shall be executed over the entire First Year.

With an ideology that the root of innovation is 'interest', the curriculum offers a wide range of elective courses - grouped into core and inter-disciplinary domains. At par with international engineering education, the students can choose to study courses concerning areas of their interests.

The curriculum introduces Skill-Based Learning (SBL), Activity-Based Learning (ABL), and Technology-Based Learning (TBL) as eXposure (SAT) courses - that assure X factor in all the students of the institute. The SAT courses shall be practiced across the first three years of engineering, focusing on graduate attributes like work ethics, responsibilities towards society, problem-solving ability, communication skills, motivation for life-long learning, leadership and teamwork, etc. that may not be copiously imbibed through regular engineering courses. The proficiencies acquired herein shall open huge employment and entrepreneurial opportunities for the students.

Students of the institute are already provided exposure to the work culture and trends in industries through live / collaborative projects / product developments, etc. Under autonomy too, through the component of Project-Based Learning included in the syllabus, the students shall develop Mini, Minor, and Major projects in Second, Third, and Last Year respectively concerning healthcare, agriculture, societal / industrial need-based problems, etc. as well as pursue internships at the end of each semester / year - making them industry-ready engineers. The blend of all these learning components in the curriculum shall strengthen the research and innovation ecosystem in the institute — for best benefits of the students.

This first syllabus shall be effective from Academic Year 2021-22 to all four years at once. It comprises 165 credits, follows the AICTE model curriculum, focuses on learner-centric approach as well as continuous evaluation, and shall offer the ideal learning experience for the students of the institute.

In the coming years, the institute shall also offer an Honours degree for students who are desirous of pursuing their special interest areas in industry-relevant tracks like Artificial Intelligence, Internet of Things, Cyber Security, etc. Through joint efforts of all stakeholders, strategic planning, and efficient execution of neoteric educational practices with hi-tech wizardry, we shall strive to become a role model for all autonomous institutes across the nation.

Dr. Suresh Ukarande
Principal and Chairman - Academic Council

Member Secretary, Academic Council's Preamble:

We, Board of Studies in Computer Engineering (CE), Information Technology (IT), Artificial Intelligence and Data Science (AI-DS), Electronics and Telecommunication (ET) and Electronics Engineering (EX) are very happy to present 4 years of undergraduate and 2 years of post-graduation in Artificial Intelligence (AI), Engineering technology syllabus effective from the Academic Year 2021-22 under the autonomy status granted to our institute, K J Somaiya Institute of Engineering and Information Technology (KJSIEIT). We are sure you will find this syllabus interesting, challenging and meeting the needs of Industry 4.0.

UGC states the benefits of granting academic autonomy to higher education institutes as the freedom to modernize curricula, making it globally competent, locally relevant and skill oriented to promote employability'. Thus exercising academic freedom by eligible and capable institutes is the need for developing the intellectual climate of our country and bringing and promoting academic excellence in higher education system. KJSIEIT under its first autonomous syllabus scheme (KJSIEIT-Scheme I) is keen in providing globally required exposure to its learners focusing sound theoretical background supported by practical experiences in the relevant areas of engineering and technology.

Besides engineering and technology foundation, Industry 4.0 demands modern, industry-oriented education, up-to-date knowledge of analysis, interpretation, designing, implementation, validation, and documentation of not only computer software and systems but also electronics and communication systems, hardware devices and tools, trained professional, ability to work in teams on multidisciplinary projects, etc. Thus KJSIEITs autonomy Scheme-I syllabus has been designed for the learners to successfully acquaint with the demands of the industry worldwide, life-long experiential learning, professional ethics with universal human values and training for needed skillsets and in line with the objectives of higher and technical education, AICTE, UGC and various accreditation and ranking agencies by keeping an eye on the technological developments, innovations, and industry requirements.

The salient features of KJSIEITs autonomy Scheme-I syllabus are:

1. Total 165 credits ensuring extra time for students' experiential learning through extracurricular activities, innovations, and research.
2. Introduction of Skill Based, Activity Based, Technology based and Project Based learning to showcase learners' creativity, interest and talent by developing additional skillsets, social involvement and contributions through activities, case studies, field visits, internships, creative learning, innovative mini, minor and major project developments, strengthen their profile and increasing the chances of employability.
3. Value addition learning through MOOCs platforms such as IBM-ICE, Coursera, NPTEL, SWAYAM, Spoken Tutorial etc.
4. Emerging areas of technology learning in Artificial Intelligence, Machine learning, Data Science, Internet of things, Cyber Security, Block chain, augmented and Virtual reality.

We would like to place on record our gratefulness to the faculty, alumni, students, industry experts and stakeholders for having helped us in the formulation of this syllabus.

Dr. Sunita R Patil

Member Secretary, Academic Council and Vice Principal, KJSIEIT, Sion

Preface by Board of Studies in Electronics Engineering:

We, the members of Board of Studies of B.Tech in Electronics Engineering are very happy to present a syllabus of Third and Last Year of B. Tech in Electronics Engineering with effect from the Academic Year 2021-22. We are assured that you will discover this syllabus interesting and challenging.

There are nine emerging technology thrust areas declared by AICTE, as an Electronics Engineer he/she should have knowledge about all the emerging technologies which will rules the industries in future so we have touched almost every emerging areas while deciding the courses and contents there in. The syllabus focuses on providing a sound theoretical background as well as good practical exposure to students in the relevant areas. Program Educational Objectives are considered while deciding different courses. It is envisioned to deliver a modern, industry-oriented education in Electronics Engineering. It aims at creating skilled engineers who can successfully acquaint with the demands of the industry worldwide. They obtain skills and experience in up-to-date knowledge to analysis, design, employ, technologies, software and systems.

At the beginning of every course we have added two theory lectures for prerequisites and course outline and at the end one theory lecture added for coverage of course conclusion which includes recap of modules, outcomes, applications, and summarization. We have mapped Course outcomes, PBL outcomes, Skills outcomes, Activity outcomes and TBL outcomes module wise throughout the syllabus. Faculty in this program adopted collaborative, co-operative and online teaching learning techniques during coverage of the course; this will help students to understand each course in depth. The designed syllabus promises to achieve the objectives of affiliating University, AICTE, UGC, and various accreditation agencies by keeping an eye on the technological developments, innovations, and industry requirements.

We would like to show our appreciation to the faculties, students, industry experts and stakeholders assisting us in the design of this syllabus.

Board of Studies in Electronics Engineering are,

Sr. No.	Name	Designation	Sr. No.	Name	Designation
1	Dr. Milind U. Nemade	Head of the Department concerned (Chairman)	9	Prof. Pankaj Deshmukh	Member
2	Dr. Sudhakar Mande	One expert to be nominated by the Vice-Chancellor	10	Prof. Sejal Shah	Member
3	Mr. Saurabh Srivastava	One Representative from Industry /Corporate Sector/ Allied area relating to Placement	11	Prof. Vidya Sagvekar	Member
4	Dr. Vaishali Wadhe	Member	12	Prof. Sheetal Jagtap	Member
5	Prof. Vrinda Ullas	Member	13	Prof. Sarika Mane	Member
6	Prof. Ganesh Wadmare	Member	14	Prof. G.R. Phadke	Member
7	Prof. Mandar Bivalkar	Member	15	Prof. Devanand Bathe	Member
8	Prof. Medha Asurlekar	Member			

Program Structure for Third and Last Year UG Technology with Credit and Examination Scheme

Program Structure for Third Year UG Technology (ET)

Semester- VI-Credit Scheme

Course Code	Course Name	Teaching Scheme (Hrs.) (TH–P–TUT)	Total (Hrs.)	Credit Assigned (TH– P–TUT)	Total Credits	Course Category
1UETC601	Basic VLSI Design	3–0–0	03	3–0–0	03	PC
1UETC602	Electromagnetic Engineering	3–0–0	03	3–0–0	03	PC
1UETC603	Computer Communication Networks	3–0–0	03	3–0–0	03	PC
1UETC604	Embedded Systems and Real Time Operating Systems	3–0–0	03	3–0–0	03	PC
1UETDLC605X	Department Level Elective-2	3–0–0	03	3–0–0	03	DLE
1UETL601	Basic VLSI Design Lab	0–2–0	02	0–1–0	01	PC
1UETL604	Embedded Systems and Real Time Operating Systems Lab	0–2–0	02	0–1–0	01	PC
1UETDLL605X	Department Level Elective-2 Lab	0–2–0	02	0–1–0	01	DLE
1UETL606	Database and Management Systems Lab	0–2–0	02	0–1–0	01	PC
1UETPR64	Project Based Learning - Minor Project Lab-2	0–2#–0	02**	0–1# –0	01	PBL
1UETXS69	Skill Based Learning-IX	0--2*--0	02	0--1--0	01	SAT
1UETXT610	Technology Based Learning-X	0--2*--0	02	0--1--0	01	SAT
Total		**15-14-0**	**29**	**15-7-0**	**22**	

PBL-Lab 2 (Preparation for Conference paper, TPP, participation in competitions, etc for Term work)

** Load of learner, not the faculty, #SAT Hours are under Practical head but can be taken as Theory or Practical or both as per the need.

Semester- VI-Examination Scheme

Course Code	Course Name	Examination Scheme								
		Marks								
		CA			ESE	TW	O	P	P& O	Total
		T1	T2	IA						
1UETC601	Basic VLSI Design	15	15	10	60	--	--	--	--	100
1UETC602	Electromagnetic Engineering	15	15	10	60	--	--	--	--	100
1UETC603	Computer Communication Networks	15	15	10	60	--	--	--	--	100
1UETC604	Embedded Systems and Real Time Operating Systems	15	15	10	60	--	--	--	--	100
1UETDLC605X	Department Level Elective-2	15	15	10	60	--	--	--	--	100
1UETL601	Basic VLSI Design Lab	--	--	--	--	25	25	--	--	50
1UETL604	Embedded Systems and Real Time Operating Systems Lab	--	--	--	--	25	25	--	--	50
1UETDLL605X	Department Level Elective-2 Lab	--	--	--	--	25	--	--	--	25
1UETL606	Database and Management Systems Lab	--	--	--	--	25	--	25	--	50
1UETPR64	Project Based Learning - Minor Project Lab-2	--	--	10	--	25	25	--	--	60
1UETXS69	Skill Based Learning-IX	--	--	--	--	20	--	--	--	20
1UETXT610	Technology Based Learning-X	--	--	--	--	20	--	--	--	20
Total		**75**	**75**	**60**	**300**	**165**	**75**	**25**	--	**775**

Minor Project 1 and 2: Students can form groups with Minimum 2 (Two) and not more than 3 (Three)

Faculty Load: 1 hour per week per four groups

Department Level Elective-2			
Group A: Data Storage and Technology	**Group B: Electronics Core**	**Group C: Artificial Intelligence and Data Science**	**Group D: Computer Domain**
1UETDLC6052	**1UETDLC6051**	**1UETDLC6053**	**1UETDLC6054**
Digital Image Processing and Machine Vision	Digital Control System	Machine Learning	Digital Design and Reconfigurable Architecture

Course Code	Course Name	Credits (TH+P+TUT)
1UETC601	Basic VLSI Design	(3+0+0)

Prerequisite:	1. Electronics Devices and circuits – I 2. Digital Logic Circuits 3. Electronics Devices and Circuits – II
Course Objectives:	1. To understand VLSI Design flow and technology trends. 2. To realize MOS based circuits using different design styles. 3. To study semiconductor memories using MOS logic. 4. To study adder, multiplier and shifter circuits for realizing data path design.
Couse Outcomes:	After successful completion of the course students will be able to: 1. Demonstrate a clear understanding of VLSI Design flow, technology trends, scaling and MOSFET models. 2. Analyze MOS based inverters. 3. Discuss different types of MOS Design styles. 4. Implement MOS based circuits using different design styles. 5. Describe semiconductor memories. 6. Realize adder, multiplier and shifter circuits using CMOS logic.

Module No. & Name	Sub Topics	CO mapped	Hrs. /Subtopic	Total Hrs./ Module
I. Prerequisite and Course Outline	Prerequisite Concepts and Course Introduction	---	02	02
1.VLSI Design flow and Technology Trends	1.1 MOSFET Scaling: Types of scaling, comparison of MOSFET Model levels, MOSFET capacitances, interconnect scaling and crosstalk, Technology Comparison: Comparison of BJT and MOS technologies	CO1	03	06
	1.2 Overview of VLSI Design Flow, Fabrication process flow of NMOS and CMOS, Lambda based design rules, Stick diagram and mask layout		03	
2. MOSFET Inverters	2.1 Introduction to MOS inverters: Active and passive load nMOS inverters, CMOS inverter and their comparison	CO2	02	08
	2.2 Static Analysis of Resistive nMOS and CMOS Inverters: Calculation of critical voltages and noise margins, Design of symmetric CMOS inverter, Layout of CMOS Inverter		04	
	2.3 Dynamic Analysis of CMOS inverter: Calculation of rise time, fall time and propagation delay, Various components of power dissipation in CMOS circuits		02	
3. MOS Circuit Design Styles	3.1 Static: Static CMOS, Pass transistor, Transmission gate, Pseudo NMOS design styles	CO3	03	05
	3.2 Dynamic: C^2MOS, Dynamic, Domino, NORA and Zipper design styles		02	
4. Combinational and Sequential	4.1 Analysis and design of 2-I/P NAND, 2-I/P NOR and complex Boolean function realization using equivalent CMOS inverter for simultaneous switching,	CO4	04	08

Circuit Realization	Layout of CMOS NAND, NOR and complex CMOS circuits.			
	4.2 Complex Boolean function realization using various design styles, Basic gates and MUX realization using pass transistor and transmission gate logic		02	
	4.3 SR Latch, JK FF, D FF, 1 Bit Shift Register realization using CMOS logic		02	
5.Semiconductor Memories	5.1 SRAM: 6T SRAM operation, design strategy, read/write circuits, sense amplifier	CO5	02	07
	5.2 DRAM: 1TDRAM, operation modes, leakage currents, refresh operation, physical design		02	
	5.3 ROM Array: NAND and NOR based ROM array		01	
	5.4 Non-volatile read/write memories: Programming techniques for flash memory, Introduction to advances in non-volatile memories: MRAM, ReRAM		02	
6. Data Path Design	6.1 Adder: CLA adder, MODL, Manchester carry chain High-speed adders: carry skip, carry select and carry save	CO6	03	05
	6.2 Multipliers and shifter: Array multiplier and barrel shifter		02	
II. Course Conclusion	Recap of Modules, Outcomes, Applications, and Summarization.	---	01	01
Total hours				42

Books:

Text Books	1. CMOS Digital Integrated Circuits Analysis and Design, Sung-Mo Kang and Yusuf Leblebici, Tata McGraw Hill, Revised 4th Edition. 2. Introduction to VLSI Circuits and Systems, John P. Uyemura, Wiley India Pvt. Ltd.
Reference Books	1. Digital Integrated Circuits: A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan Borivoje Nikolic, Pearson Education, 2nd Edition 2. Basic VLSI Design, Douglas A Pucknell, Kamran Eshraghian, Prentice Hall of India Private Ltd. 3. Logical Effort: Designing Fast CMOS Circuits, Ivan Sutherlan and Bob Sproull 4. Basics of CMOS Cell Design, Etienne Sicard and Sonia Delmas Bendhia, Tata McGraw Hill 5. CMOS VLSI Design: A Circuits and Systems Perspective, Neil H. E. Weste, David Harris and Ayan Banerjee, Pearson Education 6. Analysis and Design of Digital Integrated Circuits, David Hodges, Horace Jackson, Resve Saleh, McGraw-Hill, Inc. 7. Advanced Semiconductor Memories: Architectures, Designs, and Applications, Ashok K. Sharma, Wiley Publication 8. Magnetic Memory Technology: Spin-Transfer-Torque MRAM and Beyond, Denny D.Tang, Chi-Feng Pai, Wiley online Library 9. Resistive Switching: From Fundamentals of Nanoionic Redox Processes to Memristive Device Applications, Daniele IelMinor , Rainer Waser, Wiley online Library

Useful Links:

https://nptel.ac.in/courses/117/101/117101058/

http://cmosedu.com/

https://www.coursera.org/learn/mosfet

Assessment:

Continuous Assessment for 40 marks:

1. Test 1 – 15 marks
2. Test 2 – 15 marks
3. Internal assessment - 10 marks

Internal assessment will be based on assignments/quizzes /case study/activity conducted by the faculty

End Semester Examination will be of 60 marks for 3 hours duration.

Term work:

1. Term work should consist of a Minimum of 8 experiments.
2. Journal must include at least 2 assignments on content of theory and practical of the course "Basic VLSI Design".
3. The final certification and acceptance of term work ensures that satisfactory performance of laboratory work and Minimum passing marks in term work.
4. Total 25 Marks (Experiments: 15-marks, Attendance Theory & Practical: 05-marks, Assignments: 05-marks.

Oral: Oral examination will be based on complete syllabus.

Course Code	Course Name	Credits (TH+P+TUT)
1UETC602	Electromagnetic Engineering	(3+0+0)

Prerequisite:	1.Vector Algebra 2.Engineering Physics 3.Two Port network
Course Objectives:	1. To provide the basic skills required to understand, develop, and design various engineering applications involving electromagnetic fields. 2. To lay the foundations of electromagnetism and its practice in modern communications. 3. To provide an introduction to electromagnetic wave transmission through guided media. 4. To provide exposure to global safety standards in electromagnetic interference.
Couse Outcomes:	After successful completion of the course students will be able to: 1. Apply vector calculus to static electric and magnetic fields in different engineering situations. 2. Analyze Maxwell's equation in different forms (differential and integral) and apply them to diverse Engineering problems. 3. Analyze the phenomena of electromagnetic wave propagation in different media and in applications of Microwave engineering. 4. Analyze the nature of electromagnetic wave propagation through transmission lines. 5. Analyze different antenna structures and their applications. 6. Examine the sources of EMI and identify methods to ensure compatibility as per existing standards for electrical and electronic systems.

Module No. and Name	Sub Topics	CO mapped	Hrs. /Subtopic	Total Hrs. /Module
I. Prerequisite and Course Outline	Prerequisite Concepts and Course Introduction	---	02	02
1. Basic Laws of Electromagnetic	1.1 Qualitative interpretation of Gradient, Divergence and Curl; Coulomb's Law & Electric Field Intensity, Derivation of electric field intensity due to point, line and surface charges; Electric flux density, Gauss's Law and divergence theorem; Relationship between Electric field & Potential.	CO1	03	09
	1.2 Current and current Density, Continuity equation; Electric boundary conditions; Poisson's and Laplace's equation.		03	
	1.3 Biot-Savart's Law, Ampere's Circuital Law, magnetic field intensity of infinite current element; Magnetic flux density, Concept of magnetic scalar and vectors potentials; Magnetic boundary conditions.		03	
2. Maxwell's Equations	2.1 Faraday's law, concept of transformer and motional electromotive forces; Displacement current, Ampere's Law for time-varying fields, Maxwell's equations in differential and integral form; Concept of time varying potentials, Lorentz gauge conditions.	CO2	04	06
	2.2 Concept of phasors and time harmonic fields.		02	
3.Electromagnetic Waves	3.1 Derivation of electromagnetic wave equation, General representation of EM waves.	CO3	03	06

	3.2 Wave Propagation in Free Space, Lossy and Lossless Dielectrics and in Good Conductors, Skin Effect, Wave Polarization, Poynting's Theorem; Introduction to microwaves as an EM wave application.		**03**	
4. Transmission Lines	4.1 Transmission line parameters, Transmission line equations; Input impedance, reflection coefficient, standing wave ratio and power.	CO4	03	06
	4.2 Smith Chart, Applications of Smith Chart in finding VSWR, reflection coefficient, admittance calculations and impedance calculations over length of line. Applications of Microstrip Lines.		03	
5. Introduction to Antennas	5.1 Introduction to antennas and radiation mechanism; Basic antenna parameters: Radiation pattern, radiation power density, radiation intensity, HPBW, FNBW, directivity, Antenna radiation efficiency, Gain, bandwidth, polarization, input impedance, effective length, near and far field regions; FRIIS transmission equation.	CO5	04	09
	5.2. Types of antenna , Far-field radiating fields, radiation resistance and directivity of an infinitesimal dipole; Comparison between small dipole, finite length dipole and a half wavelength dipole; Introduction to antenna arrays; linear array of two isotropic point sources, principle of pattern multiplication; Qualitative introduction to horn antennas, reflector antennas and microstrip antennas.		04	
6. Introduction to EMI/EMC	Definition of EMI/EMC, introduction to sources and characteristics of EMI, EMI control techniques like grounding, shielding and filtering. EMC requirements for electronic systems, a review of MIL-standards, FCC and CISPR requirements.	CO6	04	03
II. Course Conclusion	Recap of Modules, Outcomes, Applications, and Summarization.	---	01	01
Total hours				42

Books:

Text Books	1. William H Hayt, John A Buck, Jaleel M. Akhtar, "Engineering Electromagnetics", 9th ed., McGraw-Hill Higher Education, 2020. 2. Matthew N. O. Sadiku, S. V. Kulkarni, "Principles of Electromagnetics", 6th ed., Oxford University Press, 2015. 3. R. K. Shevgaonkar, "Electromagnetic Waves", Tata McGraw Hill, 2005. 4. C. A. Balanis, "Antenna Theory: Analysis and Design", 4th ed., John Wiley & Sons, NJ, 2015. 5. W. Prasad Kodali, "Engineering Electromagnetic Compatibility: Principles, Measurements, Technologies and Computer Models", 2nd ed., Wiley-IEEE Press, 2001. 6. Clayton R. Paul, "Introduction to Electromagnetic Compatibility", John Wiley & Sons, 2nd ed., 2006.

Reference Books	1. John D. Kraus, Daniel A. Fleisch, "Electromagnetics: With Applications", 5th ed., Tata McGraw Hill, 2010. 2. Joseph EdMinorster, Mahmood Nahvi, "Schaum's Outline of Electromagnetics", 5th ed., McGraw Hill, 2018. 3. J. D. Kraus, R. J. Marhefka, A.S. Khan, "Antennas & Wave Propagation", McGraw Hill Publications, 5th ed., 2017. 4. R. E. Collin, "Antennas and Radio Wave Propagation", International Student Edition, McGraw Hill, 1985. Henry Ott, "Electromagnetic Compatibility Engineering", Wiley, 2009.
Useful Links:	
1. https://nptel.ac.in/courses/117/103/117103065/	
2. https://www.e-booksdirectory.com/details.php?ebook=2416	
3. https://nptel.ac.in/courses/115/101/115101005/	
4. https://www.tutorialspoint.com/electromagnetics_theory/index.asp	
5. https://kupdf.net/download/em-waves-r-s-shevgaonkar_59958a4bdc0d60da39300d1c_pdf	
6. https://engineering.purdue.edu/wcchew/ece604f19/EMFTAll20191204.pdf	
Assessment:	
Continuous Assessment for 40 marks: 1. Test 1 – 15 marks 2. Test 2 – 15 marks 3. Internal assessment - 10 marks Internal assessment will be based on assignments/quizzes /case study/activity conducted by the faculty	
End Semester Examination will be of 60 marks for 3 hours duration.	

Course Code	Course Name	Credits (TH+P+TUT)
1UETC603	**Computer Communication Networks**	**(3+0+0)**

Prerequisite:	1. Digital Communication 2. Principle of Communication
Course Objectives:	1. Introduce networking architecture like OSI and TCP/IP model and its protocols 2. Understand the various layers and protocols TCP/IP in the model . 3. Recognize different addressing schemes, connecting devices and routing protocols 4. Select the required protocol from the application layer protocols.
Course Outcomes:	On successful completion of the course the students will be able to: 1. Differentiate the working of layers in OSI model and TCP/IP model 2. Categorize physical layer services and systems. 3. Classify the various multiple access methods 4. Analyze various routing protocols in the Network layer. 5. Explain the various protocols in the Transport layer. 6. Comprehend the different protocols in application layer

Module No. & Name	Sub Topics	CO mapped	Hrs. /Subtopic	Total Hrs./ Module
I. Prerequisite and Course Outline	Prerequisite Concepts and Course Introduction	---	02	02
1.Introduction to Network Architectures, Protocol Layers, and Service models	1.1. Introduction to computer networks and its uses. LAN, MAN, WAN, Network topologies Addressing: Physical / Logical /Port addressing, Protocols and Standards.	CO1	01	04
	1.2. Protocol Architecture: Need of layered protocol architecture, Layers details of OSI, Protocol Layers and Their Service Models.		02	
	1.3.TCP/IP Model: Protocol suite, Comparison of OSI and TCP/IP		01	
2. Physical Layer	2.1. Transmission Media: Guided media like Coaxial, fiber, twisted pair, and Wireless media, Transmission Impairments. Interconnecting Devices: Hub, Bridges, Switches, Router, and Gateway.		02	06
	2.2. Introduction to LAN: LAN Protocol architecture Traditional Ethernet and IEEE 802.3 LAN Standard: Ethernet protocol, Frame structure, Physical layers, LLC, MAC layers.		02	

	2.3. Multiplexing: Synchronous TDM, Statistical TDM, ADSL		**02**	
3. Data Link Control	3.1.Data link services: Framing, Flow control, Error control, ARQ methods, Piggybacking	CO3	04	10
	3.2. High Level Data Link Control (HDLC): HDLC configurations, Frame formats, Typical frame exchanges.		02	
	3.3. Medium Access Control Protocols: ALOHA, Slotted ALOHA, CSMA, CSMA/CD , study and configuration of protocol using simulator		04	
4. Network Layer	4.1. Switching: Switched communication networks, Circuit switching networks, Circuit switching Concepts –Crossbar switch, Time Slot Interchange (TSI), TDM bus switching, Packet switching principles: Virtual circuit switching and Datagram switching.	CO4	03	10
	4.2. Routing in Packet Switching Networks: Link state Routing, Distance vector Routing. Least-Cost Routing Algorithms: Dijkstra's Algorithm, Bellman Ford Algorithm with examples and its implementation using simulator/Programming language.		04	
	4.3. Internet Protocol: IP packet, IP addressing - classful and classless, subnet and supernet addressing, IPv4, IPv6 (IPv6 Datagram format, comparison with IPv4, and transition from IPv4 to IPv6), Different IP networking Commands.		03	
5.Transport Layer	5.1. Connection –oriented Transport Protocol Mechanisms: Transmission Control Protocol (TCP): TCP Services, TCP Header format, TCP three way handshakes, Introduction of wireshark and TCP Packet Analysis using Wireshark. Connectionless transport mechanisms: User Datagram Protocol (UDP)- header format	CO5	04	06
	5.2. Congestion: Effects of congestion, Congestion control methods, Congestion control in Packet switching Networks.		02	
6. Application layer	HTTP, FTP, DNS, SMTP, Internet Telephony and Streaming Multimedia	CO6	03	03
II. Course Conclusion	Recap of Modules, Outcomes, Applications, and Summarization.	---	01	01
Total hours				42
Books:				

Text Books	1. S. Tanenbaum, "Computer Networks", Pearson Education, Fourth Edition. 2. Behrouz A. Forouzan, "Data communication and networking ", McGraw Hill Education, Fourth Edition. 3. Alberto Leon Garcia, "Communication Networks", McGraw Hill Education, Second Edition.
Reference books	1. William Stallings, "Data and Computer communications", Pearson Education, 10th Edition. 2. Computer Networking: A Top-Down Approach, by J. F. Kurose and K. W. Ross, Addison Wesley, 5th Edition. 3. Bhushan Trivedi, "Data Communication and Network", Oxford Publication Press, 1st edition.
Useful Links:	
1. https://www.nptel.ac.in	
2. https://swayam.gov.in	
3. https://www.coursera.org/	
Assessment:	
Continuous Assessment for 40 marks: 1. Test 1 – 15 marks 2. Test 2 – 15 marks 3. Internal assessment - 10 marks Internal assessment will be based on assignments/quizzes /case study/activity conducted by the faculty	
End Semester Examination will be of 60 marks for 3 hours duration.	

Course Code	Course Name	Credits (TH+P+TUT)
1UETC604	Embedded Systems and Real Time Operating Systems	(3+0+0)

Prerequisite:	1. Digital Electronics 2. Basics of Microcontrollers
Course Objectives:	1. To study concepts involved in Embedded Hardware and Software for System realisation. 2. To learn the concepts of modern microcontroller cores like the ARM-Cortex 3. To learn Real-time programming to design time-constrained embedded systems.
Couse Outcomes:	After successful completion of the course students will be able to: 1. Identify and describe various characteristic features and applications of Embedded Systems. 2. Select appropriate hardware and communication protocols for Embedded System implementation. 3. Compare GPOS and RTOS and investigate the concepts of RTOS. 4. Describe the features of Free RTOS. 5. Explain various tools for testing and debugging embedded systems 6. Design a system for different requirements based on life-cycle for an embedded system.

Module No. & Name	Sub Topics	CO mapped	Hrs. /Subtopic	Total Hrs./ Module
I. Prerequisite and Course Outline	Prerequisite Concepts and Course Introduction	---	02	02
1. Introduction to Embedded Systems	1.1 Definition, Characteristics, Classification, Applications	CO1	01	03
	1.2 Design metrics of Embedded system and Challenges in optimization of metrics		02	
2. Embedded Hardware Elements	2.1 Features of Embedded cores- µC, ASIC, ASSP, SoC, FPGA, RISC and CISC cores. Types of memories.	CO2	02	13
	2.2 Case Study: ARM Cortex-M3 Features, Architecture, Programmer's model, Special Registers, Operating Modes and States, MPU, Memory map and NVIC.		04	
	2.3 Low power - Need and techniques. Case study of Low Power modes in Cortex-M3.		01	
	2.4 Communication Interfaces: Comparative study of Serial communication Interfaces -RS-232, RS-485, SPI, I2C, CAN, USB (v2.0), Bluetooth, Zig-Bee. (Frame formats of above protocols are not expected)		04	
	2.5 Selection Criteria of Sensors and Actuators		02	
3. Embedded Software	3.1 Program Modelling concepts: DFG, CDFG, FSM.	CO3	02	12
	3.2 Real-time Operating system: Need of RTOS in Embedded system software and comparison with GPOS. Task, Task states, Multi-tasking, Task scheduling, and algorithms-Preemptive SJF, Round-Robin, Priority, Rate Monotonic Scheduling, Earliest Deadline First		10	

	Inter-process communication: Message queues, Mailbox, Event timers. Task synchronization: Need, Issues- Deadlock, Race condition, live Lock, Solutions using Mutex, Semaphores. Shared Data problem, Priority inversion.			
4. Introduction to FreeRTOS	Free RTOS Task Management features, Resource Management features, Task Synchronization features, Event Management features, Calculation of CPU Utilization of an RTOS, Interrupt Management features, Time Management features	CO4	03	03
5. Testing and Debugging Methodology	5.1 Testing & Debugging: Hardware testing tools, Boundary-scan/JTAG interface concepts, Emulator.	CO5	01	02
	5.2 Software Testing tools, Simulator, Debugger. White-Box and Black-Box testing.		01	
6. System Integration (Case Studies)	6.1 Embedded Product Design Life-Cycle (EDLC)-Waterfall Model	CO6	02	06
	6.2 Hardware-Software Co-design		01	
	6.3 Case studies for Automatic Chocolate Vending Machine, Adaptive Cruise Control , Smart Card, (highlighting i) Specification requirements (choice of components), ii) Hardware architecture iii) Software architecture)		03	
II. Course Conclusion	Recap of Modules, Outcomes, Applications, and Summarization.	---	01	01
Total hours				42

Books:

Text Books

1. Dr. K.V. K. K. Prasad, "Embedded Real Time System: Concepts, Design and Programming", Dreamtech, New Delhi, Edition 2014.
2. Rajkamal, "Embedded Systems: Architecture, Programming and Design", McGraw Hill Education (India) Private Limited, New Delhi, 2015, Edition 3rd.
3. SriramIyer, Pankaj Gupta," Embedded Real Time Systems Programming", Tata McGraw Hill Publishing Company ltd., 2003.
4. Joseph Yiu,"The Definitive guide to ARM CORTEX-M3 & CORTEX-M4 Processors", Elsevier, 2014, 3rd Edition.

Reference Books

1. David Simon,"An Embedded Software Primer", Pearson, 2009.
2. Jonathan W. Valvano, "Embedded Microcomputer Systems – Real Time Interfacing", Publisher - Cengage Learning, 2012 Edition 3rd.
3. AndrewSloss, Domnic Symes, Chris Wright," ARM System Developers Guide Designing and Optimising System Software", Elsevier, 2004
4. FrankVahid, Tony Givargis,"Embedded System Design – A Unified Hardware/Software Introduction", John Wiley & Sons Inc., 2002.
5. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, New Delhi, 2009.

Useful Links:

www.freertos.org

Assessment:

Continuous Assessment for 40 marks:

1. Test 1 – 15 marks
2. Test 2 – 15 marks
3. Internal assessment - 10 marks

Internal assessment will be based on assignments/quizzes /case study/activity conducted by the faculty

End Semester Examination will be of 60 marks for 3 hours duration.

Term work:

1. Term work should consist of a Minimum of 8 experiments.
2. Journal must include at least 2 assignments on content of theory and practical of the course "Embedded Systems and Real Time Operating Systems".
3. The final certification and acceptance of term work ensures that satisfactory performance of laboratory work and Minimum passing marks in term work.
4. Total 25 Marks (Experiments: 15-marks, Attendance Theory & Practical: 05-marks, Assignments: 05-marks.

Course Code	Course Name	Credits (TH+P+TUT)
1UETDLC6051	Digital Control System	(3+0+0)

Prerequisite:	Differential equations, Laplace transform and Matrices, Linear Control Systems
Course Objectives:	1. To introduce the discrete-time systems theory. 2. To introduce Z-transform methods in digital systems design. 3. To introduce modern state-space methods in digital systems design.
Couse Outcomes:	At the end of the course, the learner will have the ability to 1. Justify the need for digital control systems in sampling and reconstruction of analog signals. 2. Model the digital systems using various discretization methods and concept of Pulse Transfer Function. 3. Analyze the digital control systems using classical techniques. 4. Analyze the digital control systems using modern state-space techniques. 5. Design the state feedback controllers. 6. Design the state observers.

Module No. & Name	Sub Topics	CO mapped	Hrs./ Subtopic	Total Hrs. /Module
I. Prerequisite and Course Outline	Prerequisite Concepts and Course Introduction	---	02	02
1.Basics of discrete-time signals and discretization	1.1 Why digital control system? Advantages and limitations, comparison of continuous and discrete data control, block diagram of digital control system.	CO1	02	06
	1.2 Impulse sampling. Nyquist-Shannon sampling theorem, reconstruction of discrete-time signals (ideal filter)		02	
	1.3 Realizable reconstruction methods (ZOH and FOH). Transfer function of ZOH and FOH.		02	
2.Modelling of Digital Control System	2.1 Discretization Approaches: Impulse invariance, step invariance, bilinear transformation, finite difference approximation of derivative.	CO2	04	10
	2.2 Z-transform revision and its equivalence with starred Laplace transform.		03	
	2.3 The pulse transfer function (PTF) and general procedures to obtain PTF.		03	
3.Stability Analysis and Controller Design via Conventional Methods	3.1 Mapping between s-plane and z-plane, stability analysis of digital systems in z-plane. Effects of sampling frequency on stability.	CO3	03	12
	3.2 Transient and steady-state analysis of time response, digital controller design using root-locus method.		03	
	3.3 Digital controller design using bode plots, digital PID controller.		03	
	3.4 Realization of digital controllers: direct programming, standard programming, series programming, parallel programming, ladder		03	

	programming			
4.State Space Analysis of Discrete-time Systems	4.1 Revision of continuous-time state-space models. Solution of continuous- time state-space equation. Discretization of continuous-time state-space solution and discrete-time state-space model.	CO4	03	08
	4.2 Various canonical state-space forms for discrete-time systems and transformations between state-space representations.		02	
	4.3 Solution of discrete-time state-space equation. Computation of state- transition matrix (z-transforms, Caley-Hamilton theorem, Diagonalization).		03	
5.Observability and Observer Design	5.1 Concept of observability. Distinction between detectability and observability in discrete-time systems.	CO5	01	03
	5.2 Observer design (prediction observer and current observer). Output feedback controller design. Introduction to separation principle.		02	
II. Course Conclusion	Recap of Modules, Outcomes, Applications, and Summarization.	---	01	01
Total hours				42

Books:

Text Books	1. Ogata Katsuhiko, "Discrete-time Control Systems", Pearson, 2nd Edition, 1995. 2. M. Gopal, "Digital Control and State Variable Methods", Tata McGrow-Hill, 3rd Edition, 2003.
Reference Books	1. Gene Franklin, J. David Powell, Michael Workman, "Digital Control of Dynamic Systems", Addison Wesley, 3rd Edition, 1998. 2. B. C. Kuo, "Digital Control Systems", Oxford University press, 2nd Edition, 2007. 3. Chi-Tsong Chen, "Linear System Theory and Design", Oxford University Press, USA, 1998.

Useful Links:

https://nptel.ac.in/courses/108/103/108103008/

Assessment:

Continuous Assessment for 40 marks:

1. Test 1 – 15 marks
2. Test 2 – 15 marks
3. Internal assessment - 10 marks

Internal assessment will be based on assignments/quizzes /case study/activity conducted by the faculty

End Semester Examination will be of 60 marks for 3 hours duration.

Term work:

1. Term work should consist of a Minimum of 8 experiments.
2. Journal must include at least 2 assignments on content of theory and practical of the course "Digital Control System".
3. The final certification and acceptance of term work ensures that satisfactory performance of laboratory work and Minimum passing marks in term work.
4. Total 25 Marks (Experiments: 15-marks, Attendance Theory & Practical: 05-marks, Assignments: 05-marks.

Course Code	Course Name	Credits (TH+P+TUT)
1UETDLC6052	Digital Image Processing & Machine Vision	(3+0+0)

Prerequisite:	A student has to understood following subjects before learning this subject: 1. Engineering Mathematics 2. Engineering Mathematics 3. Digital Signal Processing
Course Objectives:	1. To learn the fundamental concepts of image processing for image enhancement. 2. To learn image compression, segmentation techniques with practical applications. 3. To provide basic concepts of machine vision and application development.
Couse Outcomes:	After successful completion of the course students will be able to: 1. Represent and interpret image in its numeric and graphical form. 2. Perform different image enhancement approaches for improving image quality. 3. Elucidate the mathematical modelling of image segmentation. 4. Apply the concept of image compression. 5. Explain machine vision system elements.

Module No. & Name	Sub Topics	CO mapped	Hrs./ Subtopic	Total Hrs./ Module
I. Prerequisite and Course Outline	Prerequisite Concepts and Course Introduction	---	02	02
1. Digital Image Processing Fundamentals	1.1 Introduction: Background, Representation of a Digital Image, Fundamental Steps in Image Processing, Elements of a Digital Image Processing System.	CO1	01	04
	1.2 Digital Image Fundamentals: Elements of Visual Perception, A Simple Image Model, Two dimensional Sampling and Quantization, Tonal and Spatial Resolutions, Image File Formats: BMP, TIFF and JPEG. RGB Color model.		03	
2. Enhancement in Spatial and Frequency Domain	2.1 Enhancement in the spatial domain: Negative Transformation, Power Law Transformation, Logarithmic Transformation, Gray Level Slicing (with and without background), Bit Plane Slicing, Histogram Processing, Arithmetic and logical operations on image (addition, subtraction, ANDing, ORing).	CO2	05	09
	2.2 Spatial domain filters: Smoothing Filters, Sharpening Filters, High boost filter, 2D-DFT/FFT of an image, Frequency domain image enhancement techniques.		04	
3. Image Segmentation and Morphological Operations	3.1 Relationship between pixels and connectivity, Detection of Discontinuities, Thresholding, Region based image segmentation, split and merge techniques. Image Representation and Description, Chain Code, Polygonal Representation.	CO3	07	10
	3.2 Binary Morphological Operators, Dilation and Erosion, Opening and Closing, Hit-or-Miss Transformation, Thinning and Thickening.		03	
4. Image Compression	Fundamentals: Coding Redundancy, Interpixel Redundancy, Psycho visual Redundancy Lossless Compression Techniques: Run Length Coding, Huffman Coding, Lossy Compression Techniques: Predictive	CO4	06	06

	Coding, Improved Gray Scale Quantization, Transform Coding, JPEG Standard.			
5. Machine Vision Basics	Introduction, definition, Active vision system, Machine vision components, hardware's and algorithms, Image Feature Extraction	CO5	04	04
6. Machine Vision Applications in Industry	Machine Vision for Industrial Applications, Low Angle Metal Surface (Crosshead) Inspection, Machine Vision System for Quality Grading of Painted Slates, Inspecting Glass Bottles and Jars, Stemware Inspection System, Glass Thickness Measurement Using Morphology, Inspecting Food Products		06	06
II. Course Conclusion	Recap of Modules, Outcomes, Applications, and Summarization.	---	01	01
Total hours				42

Books:

Text Books	1. Rafel C. Gonzalez and Richard E. Woods, 'Digital Image Processing', Pearson Education Asia, Third Edition. 2. S. Jayaraman, E.Esakkirajan and T. Veerkumar, "Digital Image Processing" TataMcGraw Hill Education Private Ltd, 2009. 3. Peter Corke, "Robotics, Vision and Control", Springer, 1st Edition. 4. Milan Sonka, Vaclav Hlavac, and Roger Boyle, "Image Processing, Analysis, and Machine Vision", Second Edition, Thomson Learning, 2001.
Reference Books	1. Zeuch, Nello, "Understanding and Applying Machine Vision", CRC Press; 2nd edition. 2. Bershold Klaus, Paul Holm, "Robot vision", The MIT press. 3. Bruce G. Batchelor (Ed.), "Machine Vision Handbook", Springer, 1st Edition. 4. Anil K. Jain, "Fundamentals and Digital Image Processing", Prentice Hall of India Private Ltd, Third Edition.

Useful Links:

1. https://nptel.ac.in/courses/117/105/117105079/
2. https://www.coursera.org/learn/2d-image-processing
3. https://www.edx.org/course/image-processing-and-analysis-for-life-scientists

Assessment:

Continuous Assessment for 40 marks:

1. Test 1 – 15 marks
2. Test 2 – 15 marks
3. Internal assessment - 10 marks

Internal assessment will be based on assignments/quizzes /case study/activity conducted by the faculty

End Semester Examination will be of 60 marks for 3 hours duration.

Term work:

1. Term work should consist of a Minimum of 8 experiments.
2. Journal must include at least 2 assignments on content of theory and practical of the course "Digital Image Processing & Machine Vision".
3. The final certification and acceptance of term work ensures that satisfactory performance of laboratory work and Minimum passing marks in term work.
4. Total 25 Marks (Experiments: 15-marks, Attendance Theory & Practical: 05-marks, Assignments: 05-marks.

Course Code	Course Name	Credits (TH+P+TUT)
1UETDLC6053	**Machine Learning**	**(3+0+0)**

Prerequisite:	1. Linear algebra, multivariate calculus, and probability theory 2. Neural Networks 3. Knowledge of a programming language (PYTHON/C/C ++/ MATLAB recommended)
Course Objectives:	1. Apply Machine Learning techniques in real life applications. 2. Understanding the nature of problems solved with Machine Learning. 3. Understand learning process by human and Machine learning algorithms.
Course Outcomes:	**After successful completion of the course students will be able to:** 1. Explain Machine Learning Techniques which can be used in real world scenarios. 2. Comprehend regression concept used in machine learning. 3. Explain different classification methods in machine learning 4. Apply different clustering methods that are used in machine learning. 5. Apply different optimization techniques for applications 6. Analyse Dimensionality reduction techniques.

Module No. & Name	Sub Topics	CO mapped	Hrs./ Subtopic	Total Hrs./ Module
I. Prerequisite and Course Outline	Prerequisite Concepts and Course Introduction	---	02	02
1.Introduction to Machine Learning	1.1 What is Machine Learning? Why Machine Learning?	CO1	01	06
	1.2 Examples of Machine Learning Problems, Structure of Learning, Issues in Machine Learning, Applications of Machine Learning		01	
	1.3 How to choose Right Algorithm, Steps in Developing a Machine Learning Application, Model Evaluation and Validation		01	
	1.4 Machine learning Models: Geometric Models, Logical Models, Probabilistic Models. Features: Feature types, Feature Construction and Transformation, Feature Selection		03	
2.Learning with Regression	2.1 Linear Regression, Linear basis function models, Bayesian Linear Regression, Bayesian Model Comparison	CO2	04	07
	2.2 Logistic Regression, Bayesian Logistic Regression, Naive Bay's classifier, Bayesian Belief Networks		03	

3.Learning with Classification	3.1 Classification: Rule based classification, Binary Classification, assessing classification performance, Multi-class Classification, classification by Bayesian Belief networks, Hidden Markov Models.	CO3	04	10
	3.2 Learning with Trees: Decision Trees, Constructing Decision Trees using Gini Index, Classification and Regression Trees (CART).		03	
	3.3 Support Vector Machine: Maximum Margin Linear Separators, Quadratic Programming solution to finding maximum margin separators, Kernels for learning non-linear functions.		03	
4.Clustering	4.1 K-means Clustering, Hierarchical Clustering, Expectation Maximization Algorithm, Supervised learning after Clustering, Radial Basis functions	CO4	04	08
	4.2 Case Studies: Retail store sales prediction, Credit card Fraud detection (anomaly detection), Healthcare, Telecommunications- Customer churn prediction		04	
5.Introduction to Optimization Techniques	Derivative based optimization- Steepest Descent, Newton method. Derivative free optimization- Random Search, Down Hill Simplex	CO5	04	04
6.Dimensionality Reduction:	Dimensionality Reduction Techniques, Principal Component Analysis, Independent Component Analysis, Single value decomposition	CO6	04	04
II. Course Conclusion	Recap of Modules, Outcomes, Applications, and Summarization.	---	01	01
Total hours				42
Books:				
Text Books	1. Peter Flach: Machine Learning: The Art and Science of Algorithms that Make Sense of Data, Cambridge University Press, Edition . 2. Hastie, Tibshirani, Friedman: Introduction to Statistical Machine Learning with Applications in R, Springer, 2nd Edition-2012 3. Peter Harrington "Machine Learning in Action", DreamTech Press.			
Reference books	1. Ethem Alpaydin, "Introduction to Machine Learning", PHI 2nd Edition-2013 2. C. M. Bishop : Pattern Recognition and Machine Learning, Springer 1st Edition-2013			
Useful Links:				
1. https://www.nptel.ac.in				
2. https://swayam.gov.in				
3. https://www.coursera.org/				
Assessment:				
Continuous Assessment for 40 marks:				

1. Test 1 – 15 marks
2. Test 2 – 15 marks
3. Internal assessment - 10 marks

Internal assessment will be based on assignments/quizzes /case study/activity conducted by the faculty

End Semester Examination will be of 60 marks for 3 hours duration.

Term work:

1. Term work should consist of a Minimum of 8 experiments.
2. Journal must include at least 2 assignments on content of theory and practical of the course "Machine Learning".
3. The final certification and acceptance of term work ensures that satisfactory performance of laboratory work and Minimum passing marks in term work.
4. Total 25 Marks (Experiments: 15-marks, Attendance Theory & Practical: 05-marks, Assignments: 05-marks.

Course Code	Course Name	Credits (TH+P+TUT)
1UETDLC6054	Digital Design and Reconfigurable Architecture	(3+0+0)
Prerequisite:	Digital Logic Circuits	
Course Objectives:	1.To understand, analyse & design finite state machines (FSM) 2.To train students in writing VHDL code of combinational & sequential circuits 3.To prepare students to design FSM using hardware description languages (HDL). 4. To motivate students to use reconfigurable devices for digital systems.	
Couse Outcomes:	After successful completion of the course students will be able to: 1.Analyse & design FSM. 2.Understand fundamentals of HDL and its use for designing combinational circuits. 3.Apply the concept of HDL for designing sequential circuits. 4.Develop FSM by using the fundamentals of HDL. 5.Design of complex digital systems. 6.Understand and distinguish FPGA and CPLD architecture.	

Module No. & Name	Sub Topics	CO mapped	Hrs. /Subtopic	Total Hrs./ Module
I. Prerequisite and Course Outline	Prerequisite Concepts and Course Introduction	---	02	02
1. State Machines Design	1.1 Mealy and Moore machines, Clocked synchronous state machine design, State reduction techniques, State assignment, and Clocked synchronous state machine analysis.	CO1	08	12
	1.2 Design examples on overlapping and non-overlapping sequence detector, Odd/even parity checker for serial data, vending machines.		04	
2. Introduction to VHDL	2.1 Core features of VHDL, Data types, Concurrent and Sequential statements, Data flow, Behavioral and Structural architectures, Subprograms: Function and Procedure.	CO2	03	06
	2.2 Design examples of combinational circuits like Multiplexers, De-multiplexers, Adder, Subtractor, Priority Encoder		03	
3. Design of sequential circuit using VHDL	Design examples for Flip flops, Synchronous counters, Asynchronous counters, Shift registers	CO3	04	04
4. Design of Finite State Machines (FSM) using VHDL	VHDL code for Moore, Mealy type FSMs, Serial adders, Traffic light controller, Vending machines	CO4	05	05
5. System Design using VHDL	Parallel Multiplication, Booth Multiplication, MAC unit, ALU, Memory: ROM and RAM	CO5	06	06
6. Simulation, Synthesis and Implementation	6.1 Functional simulation, Timing simulation, Logic synthesis, RTL.	CO6	03	06
	6.2 CPLD, SRAM based FPGA architecture, Spartan		03	
II. Course Conclusion	Recap of Modules, Outcomes, Applications, and Summarization.	---	01	01
Total hours				42
Books:				

Text Books	1. M. Morris Mano,"Digital Design", 5th Edition, Pearson Education India, 2012. 2. John Wakerley, "Digital Design Principles & Practices" Pearson Publication, 3rd edition. 3. Volnei A. Pedroni, "Circuit Design with VHDL" MIT Press, 2004. 4. Wayne Wolf, "FPGA Based System Design" Pearson Education. 5. W. I. Fletcher, "Engineering Approach to Digital Design" PHI publications.
Reference Books	1. R. P. Jain, "Modern Digital Electronics", 4th Edition, McGraw Hill Education, 2016. 2. Stephen Brown, Zvonko Vranesic, "Fundamentals of Digital Logic Design" McGraw Hill, 2nd edition. 3. John M. Yarbrough, Digital Logic Applications and Design, Thomson Publications, 2006. 4. P. J. Ashenden, "The students guide to VHDL" Elsevier, 1999. 5. Xilinx online resources – www.xilnix.com

Useful Links:

1. www.xilinx.com

2 https://www.youtube.com/watch?v=O3If0Nr9to0

3.https://nptel.ac.in/content/storage2/courses/117106114/week%206%20slides/6.2StateMachines2.pdf

4. https://www.youtube.com/watch?v=mwJ3uMWvJX0

Assessment:

Continuous Assessment for 40 marks:

1. Test 1 – 15 marks
2. Test 2 – 15 marks
3. Internal assessment - 10 marks

Internal assessment will be based on assignments/quizzes /case study/activity conducted by the faculty

End Semester Examination will be of 60 marks for 3 hours duration.

Term work:

1. Term work should consist of a Minimum of 8 experiments.
2. Journal must include at least 2 assignments on content of theory and practical of the course " Digital Design and Reconfigurable Architecture ".
3. The final certification and acceptance of term work ensures that satisfactory performance of laboratory work and Minimum passing marks in term work.
4. Total 25 Marks (Experiments: 15-marks, Attendance Theory & Practical: 05-marks, Assignments: 05-marks.

Lab Code	Lab Name	Credits (P+TUT)
1UETL601	Basic VLSI Design Lab	(1+0)

Lab Prerequisite:	1. Electronics Devices and circuits – I 2. Digital Logic Circuits 3. Electronics Devices and Circuits – II
Lab Objectives:	1. To understand different MOSFET models. 2. To realize MOS based circuits using different design styles. 3. To study semiconductor memories using MOS logic. 4. To study adder, multiplier and shifter circuits for realizing data path design.
Lab Outcomes (LOs):	1. Observe effect of MOSFET model level on VI characteristics. 2. Compare different MOSFET Inverters 3. Implement combinational and sequential circuits using MOS design styles. 4. Implement Memory Cell. 5. Implement adder/multiplier/shifter circuit.

Lab No.	Experiment Title	LO mapped	Hrs./Lab
I.	Lab Prerequisite	---	02
1.	To write SPICE code for obtaining Transfer Characteristics (Id-Vg) and Output characteristics (Id-Vd) of enhancement and depletion type nMOS and pMOS transistors and extract parameter like subthreshold leakage current (IL), threshold voltage (VT0) and Subthreshold Swing (SS).	LO1	02
2.	To study the impact of MOSFET scaling on the device performance.		02
3.	To study the impact of MOSFET Model parameters in Level1 / Level2 on the drain characteristics.		02
4.	To study the Voltage Transfer Characteristics (VTC) of resistive Load nMOS inverter and calculate high and low noise margins by extracting critical voltages. Also study the impact of variation of load resistance on VTC and hence on the noise margin.	LO2	02
5.	To study the effect of Kr or transistor sizing on the VTC of CMOS inverter using SPICE simulation.		02
6.	To analyse the transient performance of CMOS inverter.		02
7.	To compare performance of different types of inverters by plotting their VTCs using SPICE code.		02
8.	To realise the complex Boolean function using different design styles.	LO3	02
9.	To realize Basic gates / MUX circuits using Pass transistor /Transmission gate logic.		02
10.	To realise SR Latch, JK FF, D FF using MOS logic.		02
11.	To draw layout of CMOS inverter and extract parasitic elements.	LO4	02
12.	To draw layout of 2 input NAND/NOR gate.	LO5	02

Virtual Lab Links:

1. https://vlsi-iitg.vlabs.ac.in/
2. http://vlabs.iitkgp.ac.in/mvlsi/

Term work:

1. Term work should consist of a Minimum of 8 experiments. 2. Journal must include at least 2 assignments on content of theory and practical of the course "Basic VLSI Design". 3. The final certification and acceptance of term work ensures that satisfactory performance of laboratory work and Minimum passing marks in term work. 4. Total 25 Marks (Experiments: 15-marks, Attendance Theory & Practical: 05-marks, Assignments: 05-marks.
Oral: Oral examination will be based on experiment list and performance of experiment.

Lab Code	Lab Name	Credits (P+TUT)
1UETL604	**Embedded Systems and Real Time Operating Systems Lab**	**(1+0)**

Lab Prerequisite:	1. Basics of Microcontroller programming 2. C programming
Lab Objectives:	1. Understand Embedded IDE for practical. 2. Implementation of Embedded systems interfaces to sensors and actuators using embedded C. 3. Implementation of Free RTOS concepts. 4. Demonstration of IoT based case study.
Lab Outcomes (LOs):	After successful completion of the course students will be able to: 1. Implement embedded systems interfaces to sensors and actuators using embedded C. 2. Analyze the comparison between various serial communications interfaces used in Embedded Systems. 3. Execute Free RTOS concepts. 4. Demonstrate case study. 5. Write accurate documentation for experiments performed. 6. Apply ethical principles like timeliness and adhere to the rules of the laboratory.

Lab No.	Experiment Title	LO mapped	Hrs./ Lab
I.	Lab Prerequisite	---	02
1.	Interfacing of LEDs /switches with any embedded core. (8051/ARM/STM32, etc)	LO1, LO5, LO6	02
2.	Interfacing of Temperature sensor with any embedded core. (8051/ARM/STM32, etc)		02
3.	Interfacing of LCD/ Seven segment display with any embedded core. (8051/ARM/STM32, etc)		02
4.	Interfacing of Ultrasonic/Humidity sensor with any embedded core. (8051/ARM/STM32, etc)		02
5.	Interfacing of a relay with any embedded core. (8051/ARM/STM32, etc)		02
6.	Interfacing of a DC motor (speed and Direction control) with any embedded core. (8051/ARM/STM32,etc)		02
7.	Interfacing of a stepper motor (to move by a particular angle) with any embedded core. (8051/ARM/STM32, etc)		02
8.	Implement the I2C communication to connect to DS1307 RTC	LO 2, LO5, LO6	02
9.	Interfacing of I2C with ARM		02
10.	Interfacing of SPI with ARM		02
11.	Write a Program to Create Multiple Tasks and understand the Multitasking capabilities of RTOS(FreeRTOS).	LO3, LO5, LO6	02
12.	Simulation of multitasking using FreeRTOS		02
13.	Simulation of mutex using FreeRTOS		02
14.	Interprocess communication using Message Buffer in FreeRTOS		02
15.	Interprocess communication using queues in FreeRTOS Simulation of synchronization using Semaphore in FreeRTOS		02
16.	Embedded Systems Case Study (IA)	LO4, LO5, LO6	04

Important Note:

1. Students must perform the experiments using Simulation/Hardware.
2. Experiments must include a Minimum of 3 experiments using FreeRTOS

Term work:

1. Term work should consist of a Minimum of 8 experiments.
2. Journal must include at least 2 assignments on content of theory and practical of the course "Embedded Systems and Real Time Operating Systems".
3. The final certification and acceptance of term work ensures that satisfactory performance of laboratory work and Minimum passing marks in term work.
4. Total 25 Marks (Experiments: 15-marks, Attendance Theory & Practical: 05-marks, Assignments: 05-marks.

Oral: Oral examination will be based on experiment list and performance of experiment.

Lab Code	Lab Name	Credits (P+TUT)
1UETDLL6051	Digital Control System Lab	(1+0)

Lab Prerequisite:	Principles of Control Systems
Lab Objectives:	1. To introduce the discrete-time systems theory. 2. To introduce Z-transform methods in digital systems design. 3. To introduce modern state-space methods in digital systems design.
Lab Outcomes:	At the end of the course, the learner will have the ability to 1. Analyze the sampling and reconstruction of analog signal. 2. Model the digital systems using various discretization methods 3. Design the digital control systems using classical techniques. 4. Modelling the digital control systems using modern state-space techniques. 5. Design the controllers. 6. Design of controller and observer.

Lab No.	Experiment Title	LO mapped	Hrs./Lab
I.	Lab Prerequisite	---	02
1.	To analyse the sampling and reconstruction of analog signal.	LO1	02
2.	To study various discretization approaches (Impulse Invariance, Step Invariance, Bilinear Transformation)	LO2	02
3.	Study of time domain transient and steady-state performance and performance specifications.	LO3	02
4.	Digital controller design using Root-locus method.		02
5.	Modelling of discrete time systems in state-space and conversion to various canonical forms.	LO4	02
6.	Discrete-time system simulation in Simulink.		02
7.	Study digital PID controller and its implementation in MATLAB and Simulink.	LO5	02
8.	Controllability and Observability of discrete-time systems.		02
9.	Pole placement controller design for discrete-time systems.		02
10.	Design of deadbeat controller and observer.	LO6	02

Term work:

1. Term work should consist of a Minimum of 8 experiments.
2. Journal must include at least 2 assignments on content of theory and practical of the course "Digital Control System".
3. The final certification and acceptance of term work ensures that satisfactory performance of laboratory work and Minimum passing marks in term work.
4. Total 25 Marks (Experiments: 15-marks, Attendance Theory & Practical: 05-marks, Assignments: 05-marks.

Lab Code	Lab Name	Credits (P+TUT)
1UETDLL6052	**Digital Image Processing & Machine Vision Lab**	**(1+0)**

Lab Prerequisite:	Knowledge of a programming language (OpenCV/ Python/ MATLAB recommended)
Lab Objectives:	1.To learn basic programming skills like OpenCV, Python or Matlab 2. To enhance, segment or compress a gray level image. 3. To develop a small DIP application.
Lab Outcomes (LOs):	The students should be able to: 1. Enhance a given gray scale image 2.Apply different spatial masks on the image 3.Segment a given image 4.Develop a DIP application 5. Neatly document and submit the practical on time.

Lab No.	Experiment Title	LO mapped	Hrs./Lab
I.	Lab Prerequisite	---	02
1.	Image Enhancement	LO1, LO5	02
2.	Image Enhancement with Histogram Equalization		02
3.	Implementation of Averaging and Sharpening filters	LO2, LO5	02
4.	Edge detection using Prewitt / Sobel / Robert operator/ Laplacian of Gaussian	LO3, LO5	02
5.	Digital Image Watermarking	LO1, LO5	02
6.	Morphology Image Processing		02
7.	Image Segmentation	LO3, LO5	02
8.	Application of DIP	LO4, LO5	02

Virtual Lab Links:

1. https://cse19-iiith.vlabs.ac.in/
2. https://www.ee.iitb.ac.in/%7Eviplab/
3. https://www.ee.iitm.ac.in/ipcvlab/

Term work:

1. Term work should consist of a Minimum of 8 experiments.
2. Journal must include at least 2 assignments on content of theory and practical of the course "Digital Image Processing & Machine Vision".
3. The final certification and acceptance of term work ensures that satisfactory performance of laboratory work and Minimum passing marks in term work.
4. Total 25 Marks (Experiments: 15-marks, Attendance Theory & Practical: 05-marks, Assignments: 05-marks.

Lab Code	Lab Name	Credits (P+TUT)
1UETDLL6053	Machine Learning Lab	(1+0)

Lab Prerequisite:	1. Linear algebra, multivariate calculus, and probability theory 2. Neural Networks 3. Knowledge of a programming language (PYTHON/C/C ++/ MATLAB recommended)
Lab Objectives:	1. To Acquire advanced Data Analysis skills 2. Create ML solutions for various real life problems 3. Understanding the nature of problems solved with Machine Learning.
Lab Outcomes:	At end of successful completion of this course, student will be able to, 1. Identify machine learning techniques suitable for a given problem 2. Apply Regression Methods 3. Implement Classification method to ML application 4. Implement Clustering for ML application 5. Apply the Dimensionality Reduction Techniques

Lab No.	Experiment Title	LO Mapped	Hrs./ Lab
I.	Lab prerequisite	---	02
1.	Study of Various ML tools	LO1	02
2.	Write a program to demonstrate the working of the linear regression algorithm. Use an appropriate data set for linear regression and apply this knowledge to curve fitting on linearly separable data	LO2	02
3.	Write a program to demonstrate the working of the logistic regression algorithm. Use an appropriate data set for non-linear regression and apply this knowledge to curve fitting on non-linearly separable data.		02
4.	Write a program to demonstrate the working of the decision tree algorithm. Use an appropriate data set for building the decision tree and apply this knowledge to classify a new sample.	LO3	02
5.	Write a program to implement the naïve Bayesian classifier for a sample training data set stored as a .CSV file. Compute the accuracy of the classifier, considering few test data sets.		02
6.	Write a program to implement the SVM for a sample data set for classification. Use a Suitable data set.		02
7.	Write a program to implement PCA for the dimensionality reduction technique using a suitable data set.	LO4	02
8.	Write a program to implement Steepest Descent method to Minormize the loss function in machine learning	LO5	02
9.	Write a program to implement Random Search using a suitable data set.		02

Books:

Text Books	1.Peter Harrington ―Machine Learning In Action‖, DreamTech Press 2.Ethem Alpaydın, ―Introduction to Machine Learning‖, MIT Press 3.Tom M.Mitchell ―Machine Learning‖ McGraw Hill
Reference Books	1.Stephen Marsland, ―Machine Learning An Algorithmic Perspective‖ CRC Press 2..J.-S.R.Jang "Neuro-Fuzzy and Soft Computing" PHI 2003. 3.Samir Roy and Chakraborty, ―Introduction to soft computing‖, Pearson Edition. 4.Kevin P. Murphy , Machine Learning ― A Probabilistic Perspective

Virtual Lab Links:

1.www.ibm.com

2.https://www.coursera.org/learn/machine-learning

3.https://cedar.buffalo.edu/~srihari/CSE574/index.html

Term work:

1. Term work should consist of a Minimum of 8 experiments.
2. Journal must include at least 2 assignments on content of theory and practical of the course "Machine Learning".
3. The final certification and acceptance of term work ensures that satisfactory performance of laboratory work and Minimum passing marks in term work.
4. Total 25 Marks (Experiments: 15-marks, Attendance Theory & Practical: 05-marks, Assignments: 05-marks.

Lab Code	Lab Name	Credits (P+TUT)
1UETDLL6054	**Digital Design and Reconfigurable Architecture Lab**	**(1+0)**

Lab Prerequisite:	Basic digital logic Circuits
Lab Objectives:	1.To discuss basic concepts of Digital Design 2.To remember VHDL syntax 3. To write simple VHDL programs for simple combinational circuits. sequential circuits, FSM
Lab Outcomes (LOs):	Students should be able to: 1. Design different Finite state machines. 2. Develop combinational circuit using VHDL language 3.Develop sequential circuits, using VHDL language 4. Apply concepts of VHDL language for design of FSM. 5. Write accurate documentation for experiments performed. 6. Apply ethical principles like timeliness and adhere to the rules of the laboratory.

Lab No.	Experiment Title	LO mapped	Hrs./Lab
I.	Lab Prerequisite	---	02
1.	Design of Mealy machine	LO1,LO5,LO6	02
2.	Design of Moore machine	LO2,LO5,LO6	02
3.	Design of overlapping sequence detector		02
4.	Design of non-overlapping sequence detector	LO3,LO5,LO6	02
5.	Design of parity checker		02
6.	Write VHDL program for Multiplexors	LO4,LO5,LO6	02
7.	Write VHDL program for Demultiplexor		02
8.	Write VHDL program for adder		02
9.	Write VHDL program for subtractor		02
10.	Write VHDL program for priority encoder		02
11.	Write VHDL program for flipflop		02
12.	Write VHDL program for synchronous counters		02
13.	Write VHDL program for asynchronous counters		02
14.	Write VHDL program for shift register		02
15.	Write VHDL program for Moore, Mealy type FSM		02
16.	Write VHDL program for serial adder		02
17.	Write VHDL program for Parallel multiplication		02
18.	Write VHDL program for Booth multiplication		02

Term work:

1. Term work should consist of a Minimum of 8 experiments.
2. Journal must include at least 2 assignments on content of theory and practical of the course "Digital Design and Reconfigurable Architecture".
3. The final certification and acceptance of term work ensures that satisfactory performance of laboratory work and Minimum passing marks in term work.
4. Total 25 Marks (Experiments: 15-marks, Attendance Theory & Practical: 05-marks, Assignments: 05-marks.

Course Code	Course Name	Credits (P+TUT)
1UETL606	Database Management System Lab	(1+0)

Lab Prerequisite:	Any programming language
Lab Objectives:	1. To identify, define problem statements and construct conceptual data model for real life applications. 2. To build Relational Model from conceptual model(ER/EER). 3. To apply SQL to store and retrieve data efficiently. 4. To demonstrate notions of normalization for database design.
Lab Outcomes:	1. Identify the need of database, and define the problem statement for real life applications. 2. Create relational model for real life applications. 3. Formulate query using SQL for efficient retrieval of data. 4. Complete the term work and submit it before deadline.

Lab No.	Experiment Title	LO mapped	Hrs./Lab
I.	Lab Prerequisite	---	02
1.	Identify the case study and detail statement of problem. Design an Entity-Relationship(ER) / Extended Entity-Relationship (EER) Model & Mapping ER/EER to Relational schema.	LO1, LO4	04
2.	Create a database using Data Definition Language (DDL) and apply integrity constraints for the specified case study.	LO1, LO2, LO3, LO4	02
3.	Apply DML commands for the specified system & perform simple queries, string manipulation operations and aggregate functions		02
4.	Implement various join operations, nested and complex queries.		02
5.	Implementation of views and triggers		02
6.	Implement procedure and functions		02
7.	Use of database connectivity like JDBC		02
8.	Deploy the application		02

The case study may be chosen on any relevant topic which needs a database as backend. Suggested case studies are as follows:

- Company Database Management System
- University Database Management System
- Hospital Management System
- Student Management System
- Library Management System

Books:

Text Books	1. Korth, Slberchatz,Sudarshan, :‖Database System Concepts, 6th Edition, McGraw –Hill 2. Elmasri and Navathe, ― Fundamentals of Database Systems, 5th Edition, Pearson
Reference books	1. Peter Rob and Carlos Coronel, ― Database Systems Design, Implementation and Management, Thomson Learning, 5th Edition. 2. Raghu Ramkrishnan and Johannes Gehrke, ― Database Management Systems, TMH

Virtual Lab Links:

http://vlabs.iitb.ac.in/vlabs-dev/labs/dblab/index.php

Term work:

The case study may be chosen on any relevant topic which needs a database as backend. Suggested case studies are as follows:

1. Company Database Management System
2. University Database Management System
3. Hospital Management System
4. Student Management System
5. Library Management System

Selected case study may be divided into the following set of experiments.

1. Identify the case study and detail statement of problem. Design an Entity-Relationship(ER) / Extended Entity-Relationship (EER) Model & Mapping ER/EER to Relational schema.
2. Create a database using Data Definition Language (DDL) and apply integrity constraints for the specified case study.
3. Apply DML commands for the specified system & perform simple queries, string manipulation operations and aggregate functions.
4. Implement various join operations, nested and complex queries.
5. Implementation of views and triggers.
6. Implement procedure and functions
7. Use of database connectivity like JDBC.
8. Deploy the application.

Assignments:

1. Perform Normalization: 1NF, 2NF, 3NF.
2. Privileged database user creation.

Practical: Practical examination will be based on experiment list and performance of experiment.

Project Based Learning Code	Project Based Learning Name	Credits (P+TUT)
1UETPR64	Minor Project Lab-2	**(1+0)**

PBL Prerequisite:	**1.** Minor Project Lab- 1 2. Microcontroller Applications 3. Skill Base Lab : Python Programming
PBL Objectives:	1. To acquaint yourself with the process of identifying the needs and converting it into the problem. 2. To familiarize the process of solving the problem in a group. 3. To acquaint yourself with the process of applying HDL to attempt solutions to the problems. 4. To inculcate the process of self-learning and research.
PBL Outcomes:	Learner will be able to, 1. Identify problems and list the inputs/outputs to solve the problem 2.Draw algorithm or flowchart to solve a problem 3. Design languages such as HDL (VHDL/Verilog) 4. Install process of design board into hardware and verify it 5. Document the work done in a streamlined manner 6. Demonstrate the project on CPLD/FPGA kit. 7. Develop interpersonal skills to work as a member of a group or leader.

Module No.	Module Title	PRO mapped	Hrs./ Module
1.	Problem Definition and Project Planning: 1.1 Define a problem clearly	PRO 1	03
	1.2 Identify all the inputs required to solve the problem		
	1.3 List all the outputs of the problem		
	1.4 Gantt chart to plan the project schedule		
2.	Algorithms: 2.1 Use the structures of sequence, selection and iteration in a flowchart and pseudo code	PRO 2	03
	2.2 List the steps required to solve a problem.		
	2.3 Express these steps in the form of a pseudo code.		
	2.4 Draw a flowchart to represent the steps		
3.	Introduction to Hardware Description Language (VHDL or Verilog): 3.1 Use of design languages such as HDL (VHDL/Verilog)	PRO 3	08
	3.2 Write code for digital system design		
	3.3 Programs in VHDL/Verilog for the digital systems		
	3.4 Verification and testing of codes using software		
4.	Programming on CPLD/FPGA board: 4.1 Selection of VLSI processor (CPLD/FPGA)	PRO 4	06
	4.2 Functioning and specifying the tools used for design, as per the requirement		
	4.3 Analysis of design board		

	4.4 Installation process of design board into hardware and verify it		
	4.5 Result verification and testing		
5.	Report writing and presentation: 5.1 Document the work done in a streamlined manner preferably using LATEX	PRO 5	04
	5.2 Prepare and organise a report according to a standard format		
	5.3 Use the IEEE format of bibliography		
	5.4 Present their work using a poster		
6.	Demonstration and Poster presentation: 6.1.Demonstrate the project on CPLD/FPGA kit with result verification and testing	PRO 6, PRO 7	02
	6.2 Poster presentation		
			26

Books:

Reference Books	1. Circuit Design with VHDL(The MIT Press) Volnei A. Pedroni ,third edition 2. VHDL : A starter'Guide(2nd Edition) ,Sudhakar Yalamanchili, 3. Verilog HDL,Samir Palnitkar 4. The Verilog Hardware Description Language by Thomas & Moorby's ,fifth edition, Springer 5. Digital Design With RTL Design, VHDL, And Verilog by Frank Vahid ,2nd edition,Wiley publication 6. PLD Based Design with VHDL: RTL Design, Sythesis and Implementation, Vaobhav Taraate, Springer 7. Digital System Design with FPGAs and CPLDs by Ian Grout

Useful Links:

1. https://ieeexplore.ieee.org/
2. https://www.electronicsforu.com/
3. https://www.keil.com/
4. https://www.tinkercad.com/
5. https://www.arduino.cc/

General Guidelines:

1. Project based learning Mini Project Lab2B should be implemented using HDL programming.
2. Project is a group activity and students shall form a group of 2 to 3 students. A group shall not be more than three students.
3. Students will be assigned an open-ended problem which they will finalise according to their preferences and in consultation with the faculty supervisor.
4. Students shall submit an implementation plan in the form of Gantt/PERT/CPM chart, which will cover weekly activity of mini projects.
5. A collaborative logbook will be prepared by each group, which will be verified regularly by, guide/supervisor can verify and record notes/comments.
6. Students shall convert the best solution into working model based on HDL.
7. The solution to be validated with proper justification and report to be compiled in standard format of the college.
8. The focus of project will be on self-learning, innovation, addressing societal problems and based solutions.

Assessment:

1. The review/ progress monitoring committee shall be constituted by faculty members in-charge and/or senior faculty members.
2. The progress of the mini project to be evaluated on a continuous basis, minimum two reviews per semester. Assessment also considers peer review by students and observation of ethics.
3. Report should be prepared as per the guidelines issued by the college.
4. Minor project shall be assessed through a presentation and demonstration of working model by the student project group to a panel of examiners.
5. In the case of a major project, the evaluation will be based on fulfilment of goals by the end of semester
6. Students shall be motivated to participate in poster & project competition

Internal Assessment (10 Marks):

Internal Assessment marks should be awarded based on review/s (Quality of the problem and Clarity, Innovativeness in solutions, Cost effectiveness and Societal impact) /quiz/etc.

Term work ((25 Marks):

Distribution of Term work marks are as given below,

1. Marks awarded by guide/supervisor based on log book : 10
2. Marks awarded by review committee : 10
3. Quality of Project report : 05

Guidelines for Assessment of Minor Project Oral Examination (25 Marks):

1. Report should be prepared as per the guidelines issued by the University of Mumbai.
2. Minor Projects shall be assessed through a presentation and demonstration of working model by the student project group to a panel of Internal and External Examiners preferably from industry or research organizations having experience of more than five years approved by head of Institution.
3. Students shall be motivated to publish a paper based on the work in Conferences/students competitions.

Distribution of marks are as given below,

1. Presentation:5
2. Project Implementation:10
3. Project Report:10

Exposure (Skill Based Learning-IX) Code	Exposure (Skill Based Learning-IX) Name	Credits (P+TUT)
1UETXS69	**Linux and Networking and Server Configuration**	**(1+0)**

SBL Prerequisite:	C-Programming
SBL Objectives:	1. To install Linux and implement standard Linux commands 2. To study basic theory of Linux Operating System 3. To implement the system administrative functionality 4. To write shell script programs to solve problems 5. To study basic commands of networking 6. To develop implementation skill of different servers on Linux
SBL Outcomes:	1. Install Linux using different platforms and execute Linux commands 2. Apply the system administrative functionality and solve the problems using shell script programming. 3. Develop network based applications. 4. Apply the Linux commands using programming skills to different servers like FTP, Telnet 5. Write accurate documentation for experiments performed. 6. Apply ethical principles like timeliness and adhere to the rules of the laboratory

Module No.	Module Title	SO mapped	Hrs. /Module
1.	Linux Installation process using following method CD-ROM, Network Installation or Kickstart Installation.	SO1, SO5, SO6	02
2.	Basic commands to create users, change permission, software selection and installation and do changes in Grub file.		02
3.	Practical on configuration of Linux disk Management such as SWAP, LVM, RAID, Primary Partition, Extended Partition and Linux files system.		02
4.	Write a shell script to show various system configuration like currently logged user and his logname, your current shell, home directory, operating system type, current path setting, current working directory, show currently logged number of users, show memory information, Hard disk information like size of hard-disk, cache memory, model etc, and file system mounted.	SO2, SO5, SO6	02
5.	Write a shell script to add user and password on Linux system.		02
6.	Write a shell script to print last login details.		02
7.	Write a shell script to upgrade and cleans the system automatically instead of doing it manually		02
8.	Write a shell script to delete all log files present inside your var/log directory.		02
9.	Write a script that accepts the hostname and IP address as command-line arguments and adds them to the /etc/hosts file.		02
10.	Write a awk script to find the number of characters, words and lines in a file?		02
11.	Write a shell script that delete all lines containing a specified word		02

12.	write a shell script to find the factorial of given integer		02
13.	Configuration of DHCP Server and Client	SO3,SO 5, SO6	02
14.	Configuration of DNS Server with Domain Name.		02
15.	Configuration of NFS File server and transfer files to a windows client.		02
16.	Setting up a Samba Server and creating a print server.	SO4, SO5, SO6	02
17.	Configuration of Internet Server by creating a Proxy Server and configure browser to use as a proxy		02
18.	Configuration of Mail Server		02
19.	Configuration of Web Server.		02
20.	Configuration of FTP server and transfer files to demonstrate the working of the same		02

Virtual Lab Links:

Online Repository:

1. How to Install a DHCP Server in Ubuntu and Debian (tecmint.com)
2. How to Install and Configure Postfix as a Send-Only SMTP Server on Ubuntu 16.04 | Digital Ocean
3. Network - DHCP | Ubuntu

Books:

Text Books	1. Yeswant Kanethkar – "UNIX Shell Programming", First edition, BPB. 2. Cristopher Negus – "Red Hat Linux Bible", Wiley Dreamtech India 2005 edition.. 3. Jason Cannon ,"Linux for Beginners: An Introduction to the Linux Operating System and Command line" 4. W. Stevens, Stephen Rago , "Advanced Programming in the UNIX Environment", Addison- Wesley Professional Computing Series
Reference Books	1. Official Red Hat Linux Users guide by Redhat, Wiley Dreamtech India 2. Graham Glass & King Ables – UNIX for programmers and users, Third Edition, Pearson Education. 3. Neil Mathew & Richard Stones – Beginning Linux Programming, Fourth edition, Wiley Dreamtech India. 4. Richard Petersen, Linux: The Complete Reference, Sixth Edition

Internal Assessment (IA)

IA shall be awarded based on

1. Student's active participation in skill based learning.
2. Presenting/showcasing learned skills through Social/outreach/extension activities/Events/ Competitions/Trainings/Internships etc.
3. Submission of Report/act/demonstrations/specific participation/Idea creation/scope/creativity/Case study etc.

Assessment Rubrics	Insufficient (1)	Poor (2)	Acceptable (3)	Good (4)	Excellent (5)
Active Participation(5)					
Presentation (5)					
Report Submission(5)					
Achievement/Recognition(5)					

Exposure (Technology Based Learning-X) Code	Exposure (Technology Based Learning-X) Name	Credits (P+TUT)
1UETXT610	**1.Online Certification Courses**	(1+0)
	2.NPTEL certification	
	3.IITBs Spoken Tutorial	
	4.Swayam MOOCs	
	5.Coursera certification	
	6.Internshala Trainings	

Technology Prerequisite:	Basic Engineering and Technology courses
Technology Objectives:	1. To acquire competency in emerging areas of technology. 2. To create a mindset for life-long learning required to persist technological shifts and be abreast with the market trends. 3. To facilitate learning at self-paced schedules. 4. To boost time management ability and self-discipline. 5. To provide opportunities of strengthening digital footprints by showcasing the additional proficiency acquired as well as improve connectivity and networking. 6. To enhance employment and entrepreneurial opportunities requiring specialization.
Technology Outcomes (TOs):	1. Explain concepts of the emerging technology learned through the pursued course. 2. Describe social, ethical, and legal issues surrounding the learned technology. 3. Demonstrate professionalism and skills of digital age learning and working. 4. Demonstrate knowledge in entrance exams for higher technical education, placement interviews, and other avenues. 5. Analyze real-world case studies in society/industry for applicability of sustainable technological solutions. 6. Apply the acquired knowledge in developing technology-based solutions to real-world problems or other projects at hand.

Guidelines:

1. Learners should enrol for an online course based on their area of interest concerning emerging areas of technology in consultation with Faculty Supervisor nominated by the Head of Department.
2. The course duration should be of minimum 04 weeks.
3. Students should watch all the videos of the course to learn the course in-depth and entirety.
4. Students should solve weekly assignments that are to be submitted online within the prescribed deadline.
5. Students should register and appear for the course certification exam on scheduled date and time.
6. Students should submit the certificate of course completion to the Faculty Supervisor.
7. Faculty Supervisor shall monitor students' participation and progress at every stage — from course enrolment to certification.

Useful Links:

https://swayam.gov.in

https://www.nptel.ac.in

https://www.coursera.org

Internal Assessment (IA):

Internal Assessment shall be conducted for Total 20 Marks based on the following rubrics:

Performance Level	**Not Qualifying**	**Poor**	**Acceptable**	**Good**	**Excellent**
Marks	00	08	12	16	20
Compliance Status	Not Enrolled for any Course or Not Completed Course	Completed Course, Not Attempted Certification but Completed all Assignments.	Obtained Passing Grade or 40% of Total Score in Certification Exam **OR** Completed all Assignments with Score Above 70%.	Obtained First Class Grades or 60% of Total Score	Obtained Elite Grade or 75% of Total Score