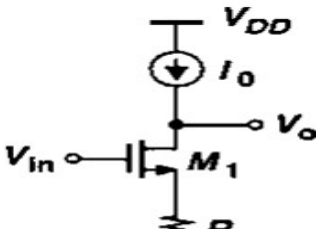
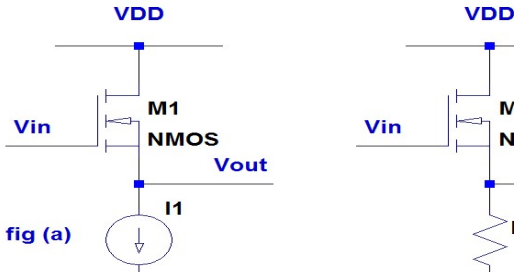
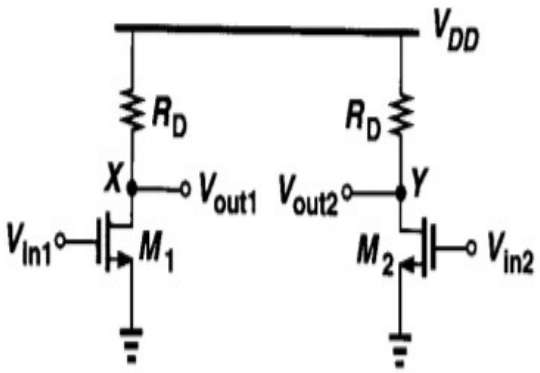
Module No.	Sr. No.	Questions along with options	Difficulty Level(S/M/D)	Answer Key a/b/c/d
1	Q.1	In Basic current mirror circuit, copied current is considered A) with channel length modulation B) without channel length modulation C) with hot electron effect D) with subthreshold conduction	M	B
1	Q.2	A Bandgap voltage reference is- A) a temperature independent voltage source B) a temperature dependent voltage source C) a pressure dependent voltage source D) a humidity dependent voltage source	S	A
1	Q.3	The "start-up" problem occurs in- A) Temperature dependent current source generation B) Temperature dependent voltage source generation C) Supply dependent current source generation D) Supply independent current source generation	D	D
1	Q.4	VBE voltage of a transistor has _____temperature coefficient A) Positive B) Negative C) Zero D) Infinity	S	A
1	Q.5	To generate temperature independent references _____are preferred A) BJT B) MOSFET C) MESFET D) MODFET	S	A
1	Q.6	Threshold voltage of n-channel MOSFET _____if body voltage drops below the source voltage A) Increase B) Decrease C) Becomes Zero D) Remains Constant	S	A

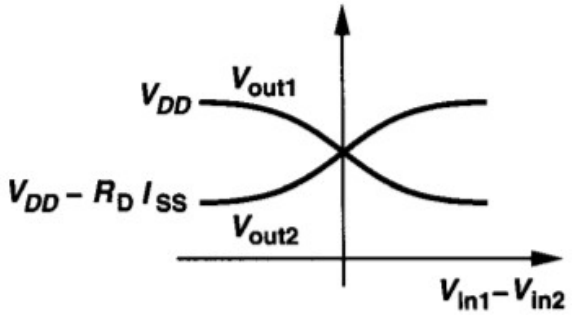
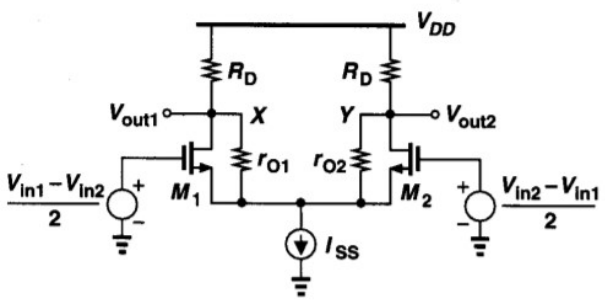
1	Q.7	What is the condition of MOSFET to operate under deep triode region? A) $V_{ds} << 2(V_{gs} - V_{th})$ B) $V_{ds} >> 2(V_{gs} - V_{th})$ C) $V_{ds} << (V_{gs} - V_{th})$ D) $V_{ds} >> (V_{gs} - V_{th})$	S	A
1	Q.8	If two bipolar transistors operate at unequal current densities, then the difference between their base-emitter voltages is A) Inversely Proportional to its Ambient Temperature B) Inversely Proportional to its Absolute Temperature C) Directly Proportional to its Ambient Temperature D) Directly Proportional to its Absolute Temperature	H	D
1	Q.9	In practical application of current mirror, early voltage is assumed to be A) Infinite B) Unity C) Zero D) Negative	S	A
1	Q.10	A current source is used A) To get high value of CMRR B) To get low voltage of gain C) To get low value of current D) To get high value of Output	M	C
1	Q.11	In CS MOSFET amplifier, the input is applied as: A) Voltage across gate and source B) Voltage across drain and source C) Current at gate D) Current at drain	S	A
1	Q.12	In MOS switch, clock feedthrough effect is also known as _____ A) charge injection B) charge feedthrough C) charge carrier D) charge ejaculation A) A & B B) B & C C) C & D D) B & D	M	A
	Q.13	In MOS devices, the current at any instant of time is _____of the voltage across their terminals.	S	C

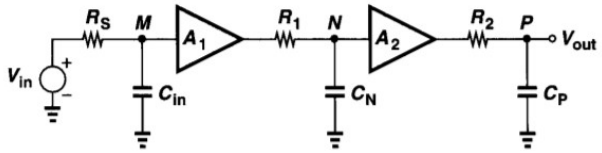
		A) constant & dependent B) constant & Independent C) variable & dependent D) variable & independent		
2	Q.14	In the below circuit if the current source is ideal, the voltage gain is:  A) $A_v = -g_m . Rs$ B) $A_v = -I_o . Rs$ C) $A_v = -g_m . Ron$ D) $A_v = -g_m/R_{on}$	D	C
2	Q.15	What is Gain of CS Amplifier with resistive load considering Channel Length Modulation? A) $- g_m R_D$ B) $- g_m r_o$ C) $- g_m (R_D \text{ ll } r_o)$ D) $- g_m (R_D + r_o)$	M	C
2	Q.16	What is the Cascode stage of Amplifier? A) CS+CD B) CS+CG C) CD+CG D) CS+CS	S	B
2	Q.17	Which configuration is useful for the application which needs low input impedance? A) Common Source Amplifier with Resistive Load B) Common Gate Amplifier C) Common Source Amplifier with current source load D) Common Drain Amplifier	M	B
2	Q.18	Among listed which Configuration provides higher voltage gain? A) CS Amplifier with current source load B) CS Amplifier with source degeneration C) CS Amplifier with Diode connected load D) CS Amplifier with Triode Load	S	A
2	Q.19	In Common Source Stage with Diode connected load, MOSFET used as load operate in: A) Saturation Region	S	A

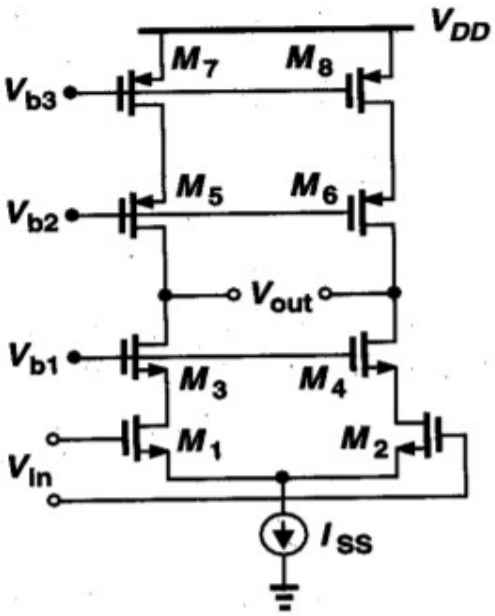
		B) Linear Region C) Deep Triode Region D) Cut off region		
2	Q.20	Which type of amplifier is a source follower? A) Common Source Amplifier B) Common Drain Amplifier C) Common Gate Amplifier D) Common Collector Amplifier	S	B
2	Q.21	The main advantage of Cascode configuration is _____ A) High Bandwidth B) Low output resistance C) High input resistance D) Low Bandwidth	M	A
2	Q.22	In a common source amplifier circuit if the source resistance R_s is shorted the gain of the Amplifier A) Increased B) Decreased C) Remain Constant D) Zero	S	A
2	Q.23	The differential gain equation of basic differential pair with resistive load is _____ A) $g_m^2R_D$ B) $-g_{m.}$ RD C) $g_mR_D^2$ D) $-g_m^2R_D$	S	B
2	Q.24	The center potential in differential signalling is called as the_____ A) Offset voltage level B) Threshold voltage level C) Common Mode level D) Differential voltage level	S	C
2	Q.25	The Thermal noise in amplifier Increases with _____ A) Increase in frequency B) Increase in temperature C) Decrease in frequency D) Decrease in temperature	S	B
2	Q.26	In a Cascode current source the O/P resistance can be increased by cascading transistors in _____. A) Series with each other B) Parallel with each other C) Parallel with series	M	A

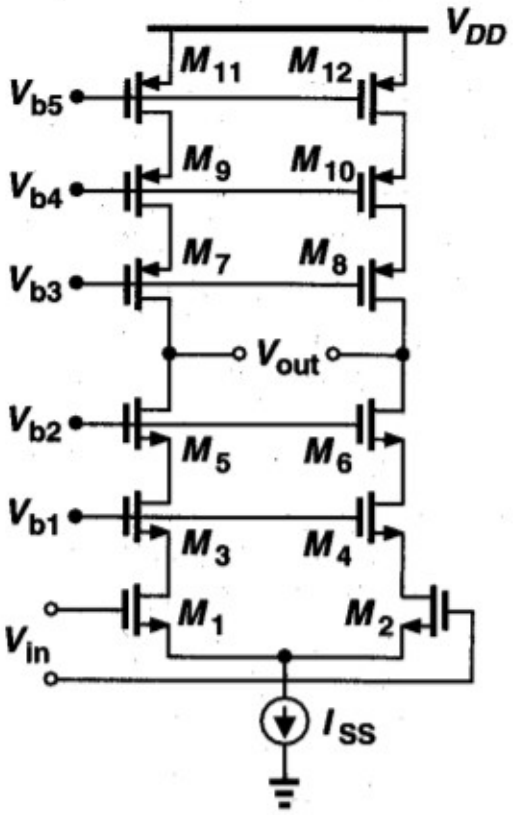
		D) Series with parallel		
2	Q.27	For the Common Drain stage configurations shown in fig(a) and fig(b) the respective voltage gains are given by  A) (gm. Rs)/[1+(gm+gmb) Rs] and gm/(gm+gmb) B) gm/(gm+gmb) and (gm. Rs)/[1+(gm+gmb) Rs] C) $g_m r_o$ and $g_m Rs$ D) Infinity and Zero	D	**B**
2	Q.28	Operating modes of Differential Amplifier? A) Common Mode B) Differential Mode C) Absolute Mode D) Common Mode, Differential Mode	S	D
3	Q.29	Which is not a performance parameter of Op-amp? A) Non-linearity B) Gain C) Noise and offset D) Small signal bandwidth	S	A
3	Q.30	In 2-stage Op-amp topology, each stage provides- A) High gain, High impedance B) High gain, High swing C) High impedance, High gain D) Low impedance, High swing	S	B
3	Q.31	Which Op-amp topology gives highest speed and low power dissipation? A) Telescopic Op-amp B) Two-stage Op-amp C) Folded Cascode Op-amp D) Gain boosting	M	A
3	Q.32	Drawback of Telescopic Cascode Op-amp is- A) limited gain B) low speed C) high power dissipation	S	D

		D) Limited output swing and difficulty in shorting I/p and O/p.		
3	Q.33	Which Op-amp topology do not require addition of more transistors to increase gain? A) Telescopic Op-amp B) Two-stage Op-amp C) Folded Cascode Op-amp D) Gain boosting	M	D
3	Q.34	Which Op-amp topology have low speed in operation? A) Telescopic Op-amp B) Two-stage Op-amp C) Folded Cascode Op-amp D) Gain boosting	S	B
3	Q.35	The problem with the single operational difference amplifier is its A) High input resistance B) Low input resistance C) High output resistance D) Low output resistance	S	B
3	Q.36	If for an amplifier V1 and V2 are the input signals, Vc and Vd represent, the common mode and differential signals respectively, then the expression for CMRR which is not correct, A) 20 log ($\|A_d\| / \|A_c\|$) B) -10 log (|Ac| / |Ad|)2 C) 20 log (v2 – v1 / 0.5(v2 + v1)) D) 5 log (V2/V1)	D	D
3	Q.37	Following diagram depicts the circuit of  A) Basic Differential Pair B) Cascode amplifier C) CD stage amplifier D) CG stage amplifier	D	A

3	Q.38	To increase the input resistance in differential amplifier, replace the tail transistor by A) Current mirror B) Amplifier C) Oscillator D) CS stage amplifier	M	A
3	Q.39	What is CMRR? A) A_c/A_d B) A_d/A_c C) A_d D) A_c	S	B
3	Q.40	Following is the ----------characteristics of differential pair  A) Input B) Output C) Input Output D) high impedance	S	C
3	Q.41	In this circuit shown in figure the current drawn from M1 and M2 is equal to  A) Iss/2 B) Iss/3 C) Iss/4 D) Iss/5	S	A
3	Q.42	As a standard approach, the phase margin while	S	B

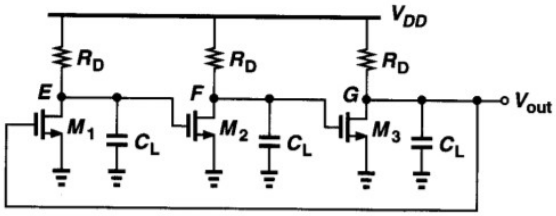
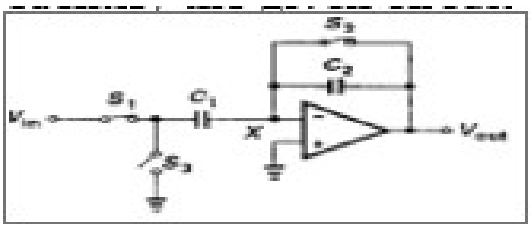
		designing two stage opamp should be at least_____ A) 90° B) 45° C) 30° D) 70°		
3	Q.43	Which among the following causes common mode response in differential pairs? A) Match in Transistor B) Mismatch in Transistors C) Match in Resistors D) Infinite resistance of tail current source	M	B
3	Q.44	In a two-stage op-amp, what is the purpose of compensation circuitry? A) To provide high gain B) To lower output resistance & maintain large signal swing C) To establish proper operating point for each transistor in its quiescent state D) To achieve stable closed-loop performance	S	D
3	Q.45	Name the circuit shown in figure  A) Cascode of amplifiers B) Darlington pair C) Cascade of Amplifiers D) Single stage amplifiers	S	C
3	Q.46	The most important advantage of differential signalling over single ended signalling is _____ A) Reduction in noise B) Increase in Gain C) Reduction in Gain D) Increase in Slew Rate	S	A
3	Q.47	For two stage opamp with 60° phase margin, the relation between compensation capacitor (Cc) and load capacitor (CL) is_____ A) $C_C \geq 0.22\ C_L$ B) $C_C \geq 0.1$ CL C) $C_C \leq 0.22\ C_L$ D) $C_C \leq 0.1$ CL	M	A
3	Q.48	A single common source stage does not oscillate if it is placed in unity gain loop, because of-	M	B

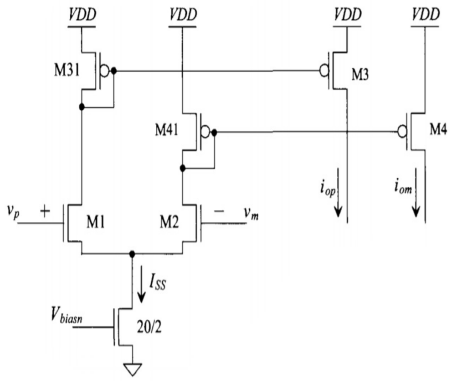
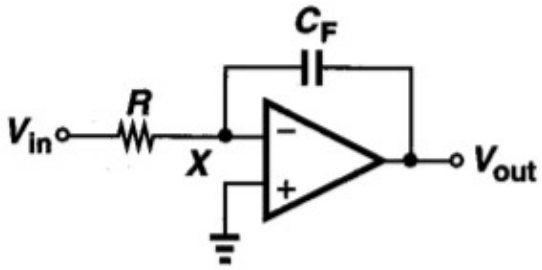
		A) maximum phase shift of 180 degree B) maximum phase shift of 270 degree C) maximum phase shift of 360 degree D) no phase shift		
3	Q.49	The circuit shown in figure is  A) Single stage opamp B) Differential amplifier C) Current Mirror D) Cascode op-amp	M	D
3	Q.50	Following circuit is	D	A

		 A) Triple cascode opamp B) Double cascode opamp C) Single cascode opamp D) Differential Amplifier		
3	Q.51	PSSR can be defined as the product of the ratio of change in supply voltage to change in output voltage of op-amp caused by the change in power supply & _____ of op-amp. A) Open-loop gain B) Closed-loop gain C) Forward Gain D) Feedback gain	M	A
3	Q.52	Which of the following is not a boundary constraint while designing an OpAmp? A) Technology Node B) Supply Voltage and current C) Operating temperature D) Slew rate	S	D
3	Q.53	In a two stage opamp Miller theorem can be used for which of the following? A) To convert floating impedances to grounded impedances. B) To calculate current flowing through a loop	M	A

		C) To calculate voltage across a component in an electrical network. D) Calculate the gain of the circuit		
3	Q.54	OPAMP is often called as _____ A) CS Amplifier B) CD Amplifier C) High gain differential amplifier D) Low gain differential amplifier	S	C
3	Q.55	Which of the following parameters is used to determine the noise performance of a differential amplifier? A) ICMR B) Gain C) CMRR D) Slew Rate	S	C
3	Q.56	With zero volt on both inputs a differential amplifier should ideally have an output A) Equal to positive of the supply voltage. B) Equal to negative of the supply voltage. C) Equal to Zero D) Equal to CMRR	S	C
4	Q.57	Which one is true for Full Custom Design? A) simple in design B) low cost C) require more time to design D) require less time to design	M	C
4	Q.58	Which one is true for Semi Custom Design? E) Difficult in design F) high cost G) require less time to design H) require more time to design	M	C
4	Q.59	Select the correct option about the relation between sensitivity of voltage-controlled oscillator and supply voltage of the system. A) Sensitivity increases as supply voltage increases B) Sensitivity decreases as supply voltage increases C) Sensitivity not affected by change in supply voltage D) Sensitivity exponentially increases as supply voltage increases	M	B
4	Q.60	In which design all circuitry and all interconnections are designed? A) gate array design B) semi-custom design	S	C

		C) full custom design D) transistor design		
4	Q.61	Select the option which is not correct about DLL over PLL. A) DLLs are more susceptible to noise. B) DLLs are more stable. C) DLLs don't have settling issues. D) DLLs are less susceptible to noise	M	A
4	Q.62	Which circuit is used to eliminate skew in PLL? A) Buffer B) Buffer and Capacitor C) Capacitor D) Buffer and Amplifier	M	B
4	Q.63	Give the Combination of basic blocks of PLL A) VCO, LPF, PD B) LPF, VCO, PD C) LPF, PD, VCO D) PD, LPF, VCO	S	D
4	Q.64	Which circuit is used to increase the acquisition range of PLL? A) Net pump PLL B) Charge pump PLL C) PLL D) DLL	M	B
4	Q.65	Application of PLL? A) Frequency Compensation B) Voltage Multiplier C) Frequency Multiplication D) Current Multiplier	S	C
4	Q.66	An LC oscillator may be realized with a _____ transistor in the signal path. A) Minimum two B) Minimum three C) Minimum four D) Only one	S	D
4	Q.67	An ideal voltage-controlled oscillator is a circuit whose A) Output voltage is linear function of its control input voltage B) Output frequency is linear function of its control input voltage C) Output frequency is linear function of its control input frequency D) Output voltage is linear function of its control input frequency	M	B

4	Q.68	The aligning of output phase of voltage-controlled oscillator with reference is called: A) Phase compensation B) Phase alignment C) Phase Locking D) Phase detecting	S	C
4	Q.69	The below shown oscillator circuit is  A) Three stage ring oscillator B) Two stage ring oscillator C) Single stage ring oscillator D) Differential pair	D	A
5	Q.70	The speed of operation and greater voltage swings of a MOSFET sampling circuit achieved A) In only NMOS sampling circuit B) In only PMOS sampling circuit C) Parallel combination of NMOS and PMOS sampling circuit D) Series combination of NMOS and PMOS sampling circuit	S	C
5	Q.71	Identify the given circuit of switched capacitor  A) Inverting amplifier B) Noninverting amplifier C) Integrator D) Sample and hold amplifier	S	B
5	Q.72	The comparator consists of stages in sequence: A) Preamplification/ Decision circuit/ Postamplification B) Decision circuit /Preamplification/ Postamplification C) Decision circuit /Preamplification/ Postamplification/flipflop D) Preamplification /Decision circuit /	S	A

		Postamplification/ flipflop		
5	Q.73	The figure given below is preamplification stage of comparator where the sizes of MOSFET M1 and M2 are set by  A) The diff-amp transconductance, gm, and the input capacitance B) Input common mode voltage and the input capacitance C) Input common mode voltage and output voltage swing D) The diff-amp transconductance, gm, and input common mode voltage	D	A
5	Q.74	Below circuit shown is  A) Switched Capacitor Integrator B) Switched Capacitor Differentiator C) Adder D) Subtractor	S	A
5	Q.75	The primary advantage of switched capacitor circuit is_____ A) Non Compatibility with CMOS technology B) Good accuracy of time constants C) Less voltage linearity D) Less switching capacity	S	B
5	Q.76	The primary disadvantage of switched capacitor circuits is _____ A) Clock feedthrough	M	D

		B) less Necessity of bandwidth of the signal being less than the clock frequency C) Consumes more space D) Clock skew		
5	Q.77	What is PTAT A) Proportional to absolute Temperature B) Proportional to different Temperature C) Proportional to complete Temperature D) Phase to absolute Temperature	S	A
5	Q.78	Which among the following can be regarded as the application of MOS switch in an IC design? A) Modulation B) Gates in digital circuits C) Simulation of a resistor D) Demodulation	M	B
6	Q.79	Suppose you had a thermometer with only two readings, hot and cold, So how many quantisation levels? A) 3 B) 4 C) 1 D) 2	S	D
6	Q.80	Typical error associated with an S/H circuit in acquisition time A) Pedestal error B) Droop C) Overshoot and settling time D) feedthrough	M	C
6	Q.81	Consider a 3-bit DAC with $V_{ref} = 5$ V, then the value of LSB is given by A) 1.66V B) 0.625V C) 1.66V D) 0.625V	M	B
6	Q.82	Consider a 3-bit DAC with $V_{ref} = 5$ V, then the accuracy is given by A) 12.50% B) 0.39% C) 0.00% D) 0.63%	D	A
6	Q.83	A binary input 000 is fed to a 3-bit DAC/ADC, the resultant output is 101. Find the type of error? A) Settling error B) Gain error C) Offset error D) Linearity error.	M	C
6	Q.84	A monotonic DAC is one whose analog output	M	C

		increases for A) Decrease in digital input B) An increase in Analog input C) An increase in Digital input D) Decrease in Analog input.		
6	Q.85	A circuit which is used as a sampling gate in data converters A) Sample Circuit B) Hold Circuit C) Sample and Hold Circuit D) Schmitt Trigger	M	C
6	Q.86	An ADC which contain sample and hold circuit, Mux and shift register? A) Successive Approximation ADC B) R-2R Ladder ADC C) Cyclic ADC D) Flash ADC	S	C
6	Q.87	Which DAC uses resistor? A) String DAC B) Flash ADC C) Successive Approximation ADC D) Cyclic DAC	S	A
6	Q.88	Which ADC has highest accuracy? A) R-2R DAC B) Flash DAC C) Successive Approximation DAC D) Cyclic DAC	S	C
6	Q.89	Which is the fastest ADC type? A) R-2R ADC B) Flash ADC C) Successive Approximation ADC D) Cyclic ADC	S	B
6	Q.90	10-bit ADC form how many bits number? A) 8-bit Number B) 10-bit Number C) 16-bit Number D) 12-bit Number	S	B
6	Q.91	ADC resolution given by. A) 2^{n-1} Output Codes B) 2^{2n+1} Output Codes C) 2^{n} Output Codes D) 2^{n-1} Output Codes	M	C
6	Q.92	What is the LSB of 16-bit ADC? A) One part 65,000 B) One part 64,536	M	C

		C) One part 65,536 D) One part 65,500		
6	Q.93	Anti-aliasing filter is used in _____ A) A to D conversion before ADC B) D to A conversion before DAC C) A to D conversion after ADC D) D to A conversion after DAC	M	A
6	Q.94	Analog to Digital Converter (ADC) which does not use Digital to Analog Converter (DAC) is _____ A) Dual slope integrator ADC B) Successive approximation ADC C) Staircase ramp ADC D) All of the above	M	A
6	Q.95	The main drawback of dual slope integrator type ADC is it's_____ A) Slow conversion time B) High cost C) Low sensitivity D) Temperature immunity	M	A
6	Q.96	For accurate sampling of signal with maximum frequency(f_m), the sampling frequency ($s_{ampling}$) in sample and hold circuit should be at least_____ A) 5 f_m B) $2f_m$ C) 1.2 f_m D) $0.5f_m$	S	B
6	Q.97	The fastest Analog to Digital Converter (ADC) is_____ A) Single slope type ADC B) Dual slope integrator type ADC C) Successive approximation ADC D) Counter type ADC	M	C
6	Q.98	Digital to analog conversion cannot be done by_____ A) Weighted resistor method B) R-2R ladder C) Inverted R-2R-ladder method D) Flash type ADC	S	D
6	Q.99	A simple resistor string 3-bit DAC composed of A) 8 identical resistors and 3 switches B) 3 identical resistors and 8 switches C) 3 identical resistors and switches	M	D

		D) 8 identical resistors and switches		
6	Q.100	The maximum deviation between actual and ideal converter output after the removal of error is A) Absolute Accuracy B) Relative Accuracy C) Linearity Accuracy D) Nonlinearity Accuracy	M	B